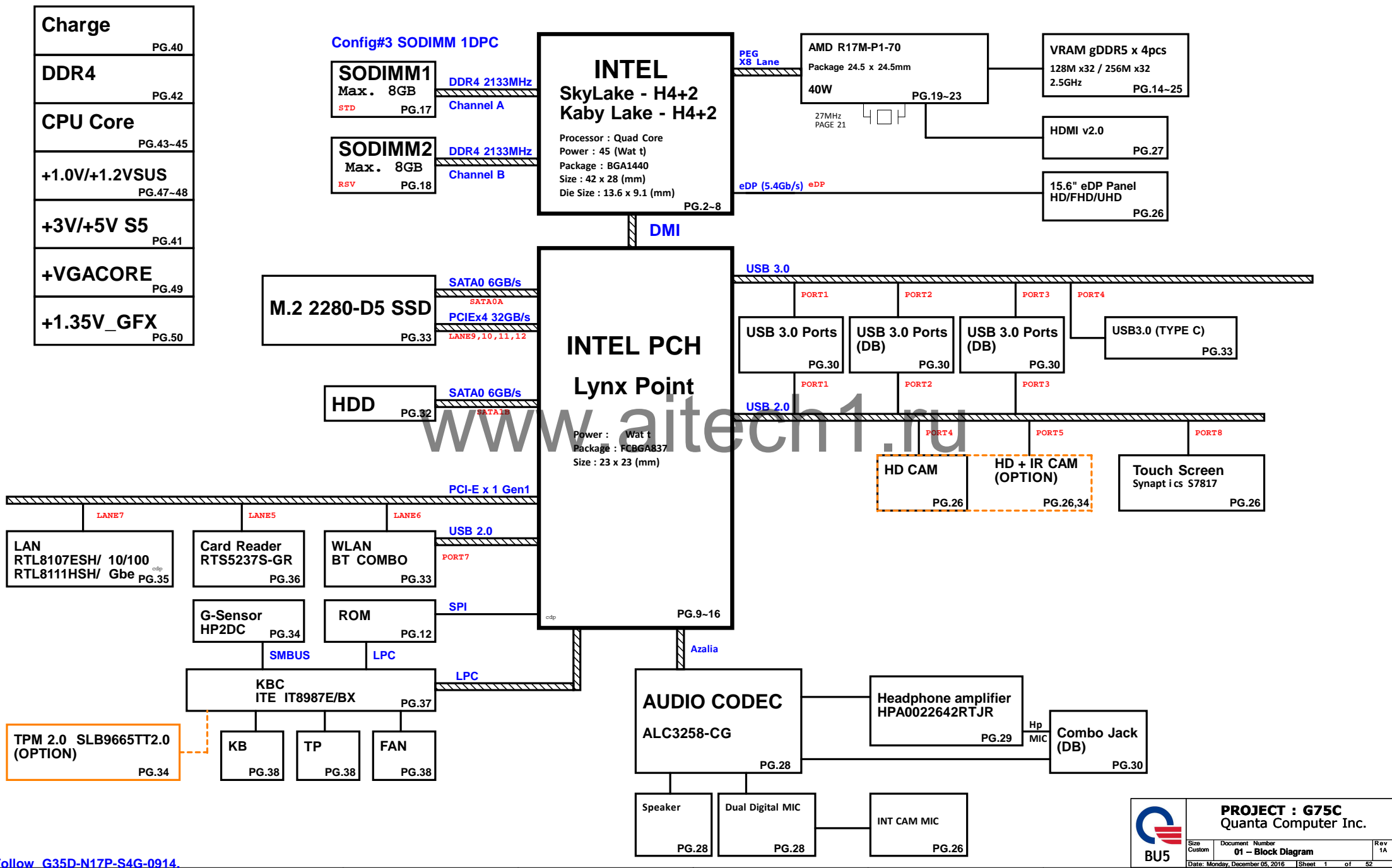
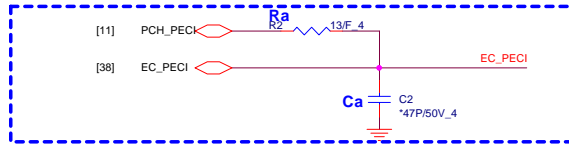


# POWER PAVILION INTEL SKL / KABY -H SYSTEM DIAGRAM

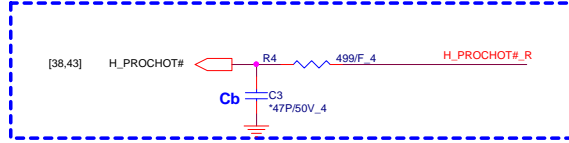
01



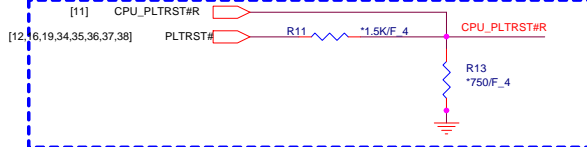
**H\_PECI (50ohm)**  
Trace Length: <0.5 inches  
Ra,Ca need placement close to PCH.



**PROCHOT# (50ohm)**  
Trace Length <11 inches  
Cb need placement near VR

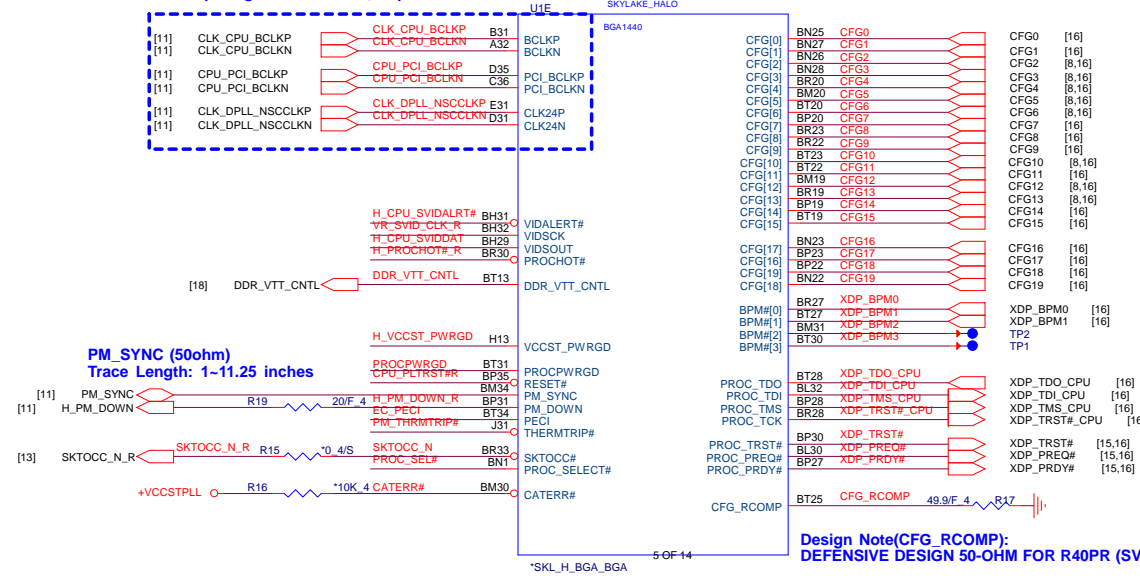


**CPU\_PLTRST# (50ohm)**  
Trace Length: 10~17 inches

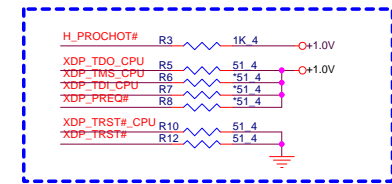


## SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedance 90 ohm



## Processor pull-up (CPU)



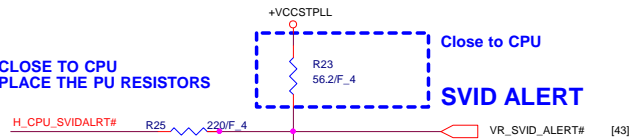
## CPU CORE SVID

Layout note:  
1.Need routing together  
2.ALERT need between CLK and DATA.

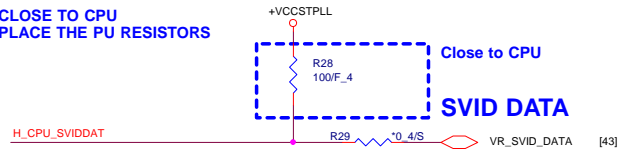
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



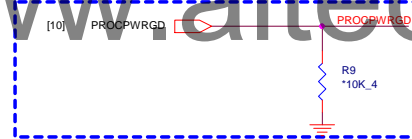
CLOSE TO CPU  
PLACE THE PU RESISTORS



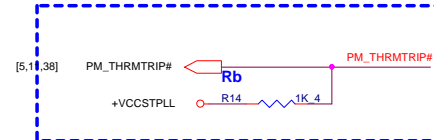
CLOSE TO CPU  
PLACE THE PU RESISTORS



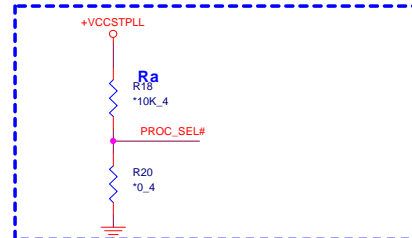
**PROC\_PWRGD (50ohm)**  
Trace Length: 1~11.25 inches



**THERMTRIP# (50ohm)**  
Trace Length: 1.1~12 inches  
Rb need placement near PCH

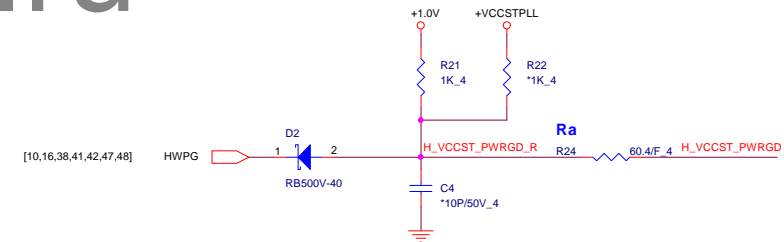


**Ra(R10804) Not install in SKL-H**



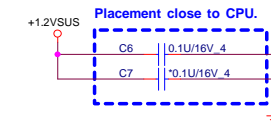
## HWPD

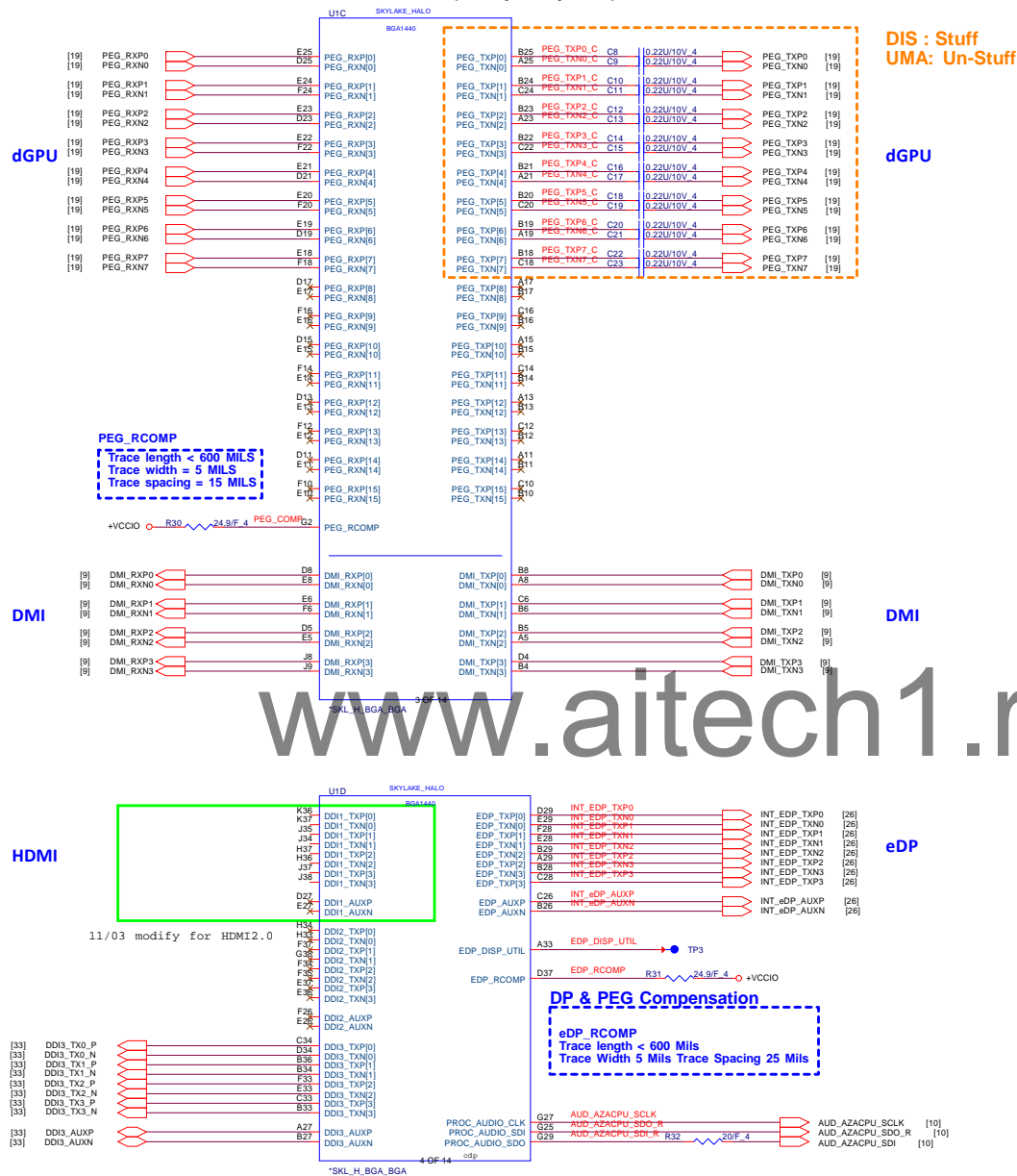
Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"



## CPU VDDQ

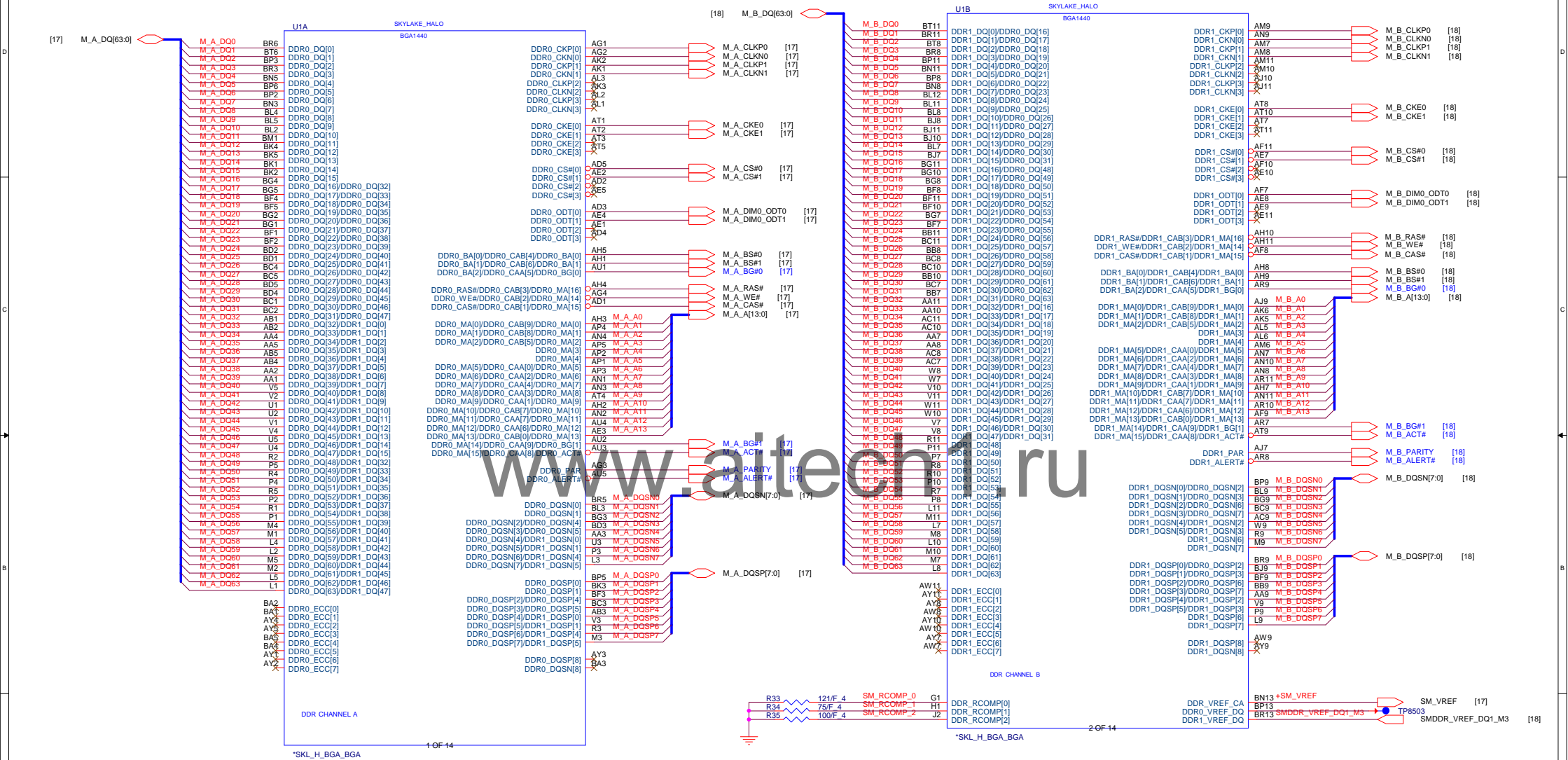
Note: please keep plane is enough for VDDQ 2.8A





+1.2VSUS [2,6,10,17,18,42,48]  
+3VSS [10,12,14,30,33,34,38,41,42,44]  
+3V [5,8,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,37,38,39,40,43,45,46,47,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,90,91,92,93,94,95,96,97,98,99,100]

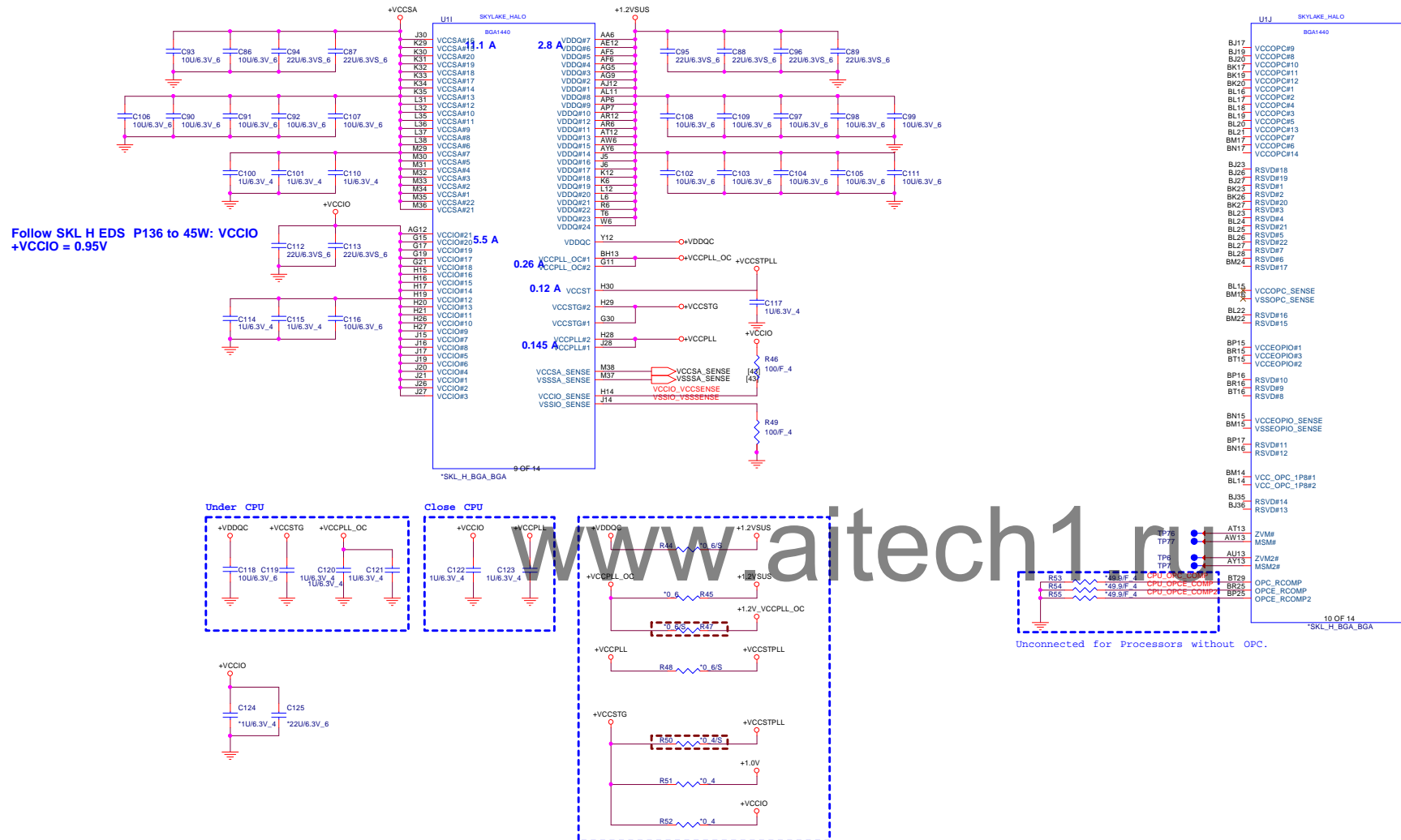
## SKYLAKE Processor (DDR4)

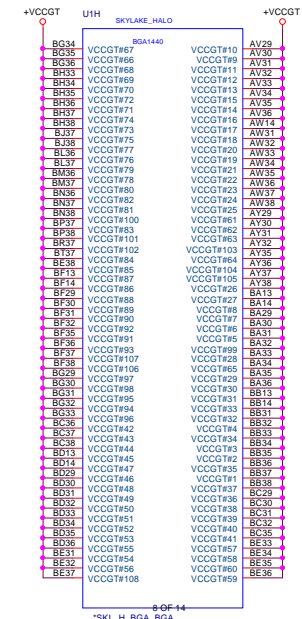






Follow SKL H EDS page 135 45W: VDDQ=2.8A





Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm

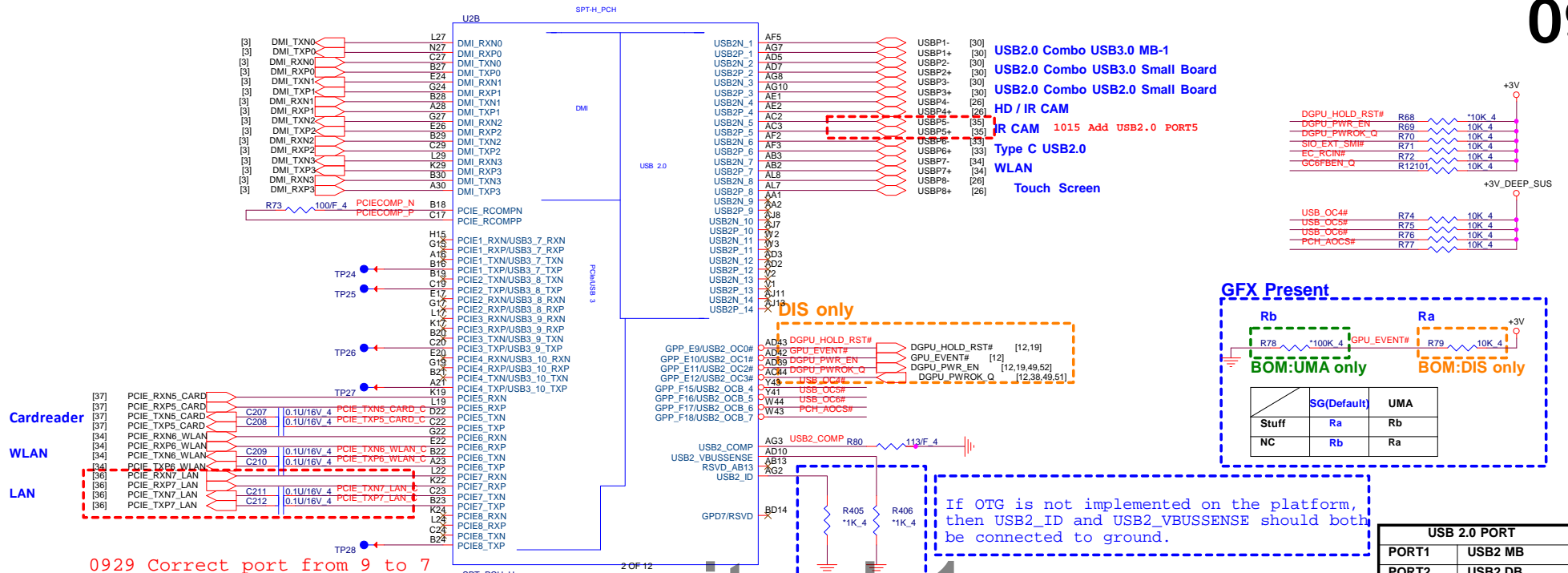
 +VCC\_CORE [43,44]



Size Custom	Document Number 07 -- SKL 6/7 (POWER&GND )	Re 1
Date: Monday, December 05, 2016	Sheet 7 of 52	

SKL-HProcessor (GND)





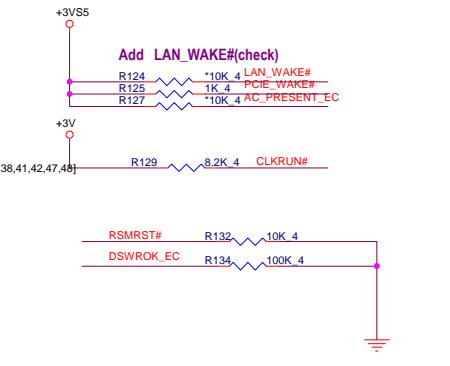
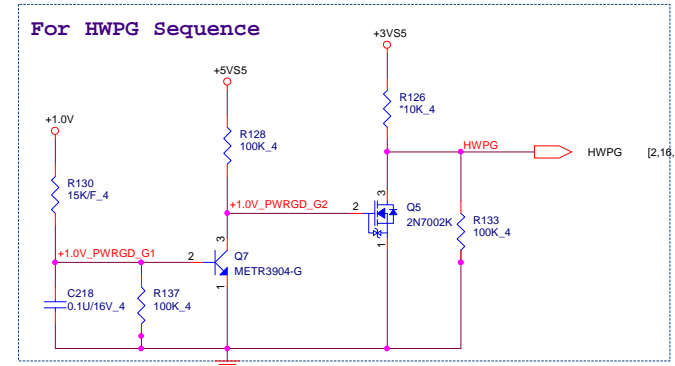
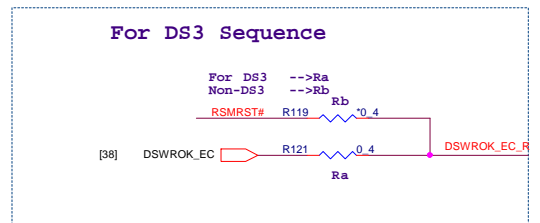
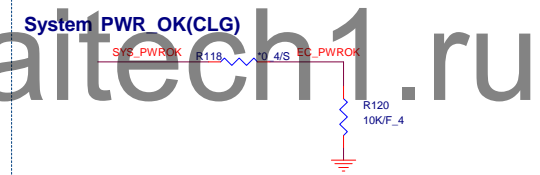
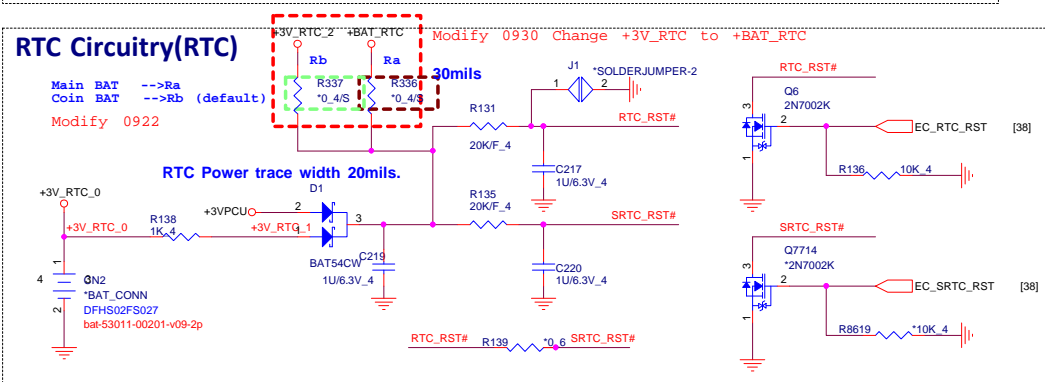
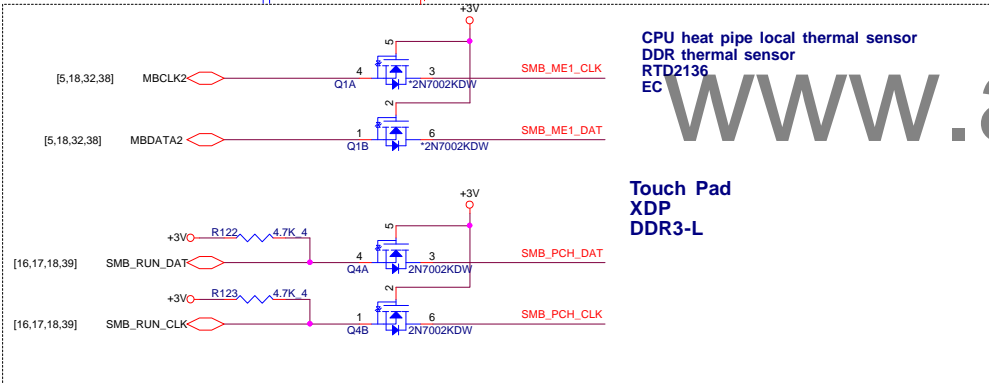
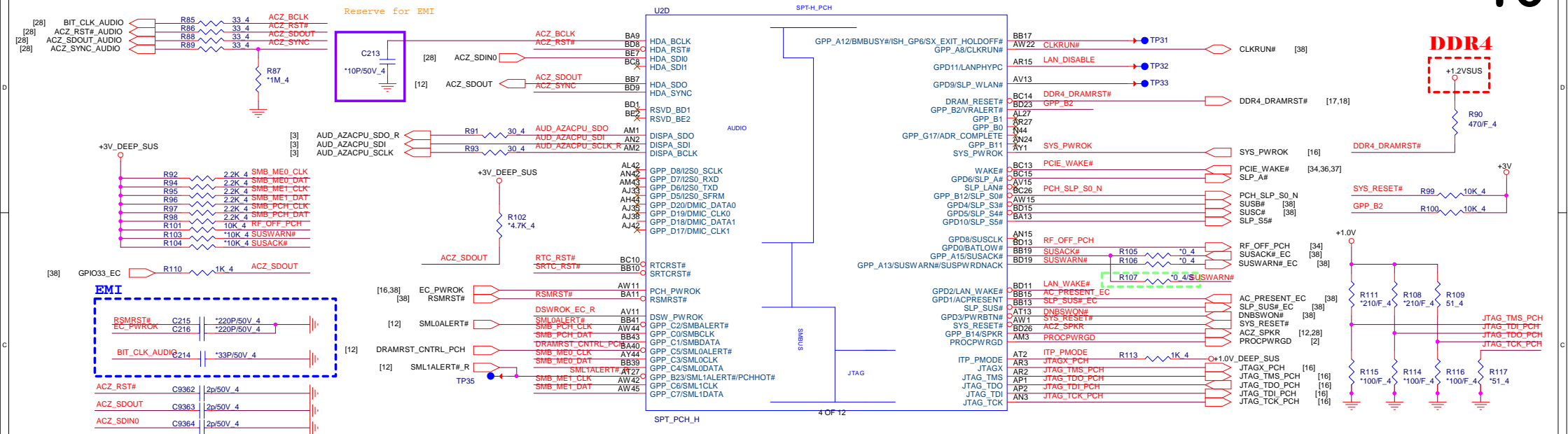
**USB3.0 (M/B-1)**

**USB3.0 (Small Board)**

**USB3.0 (Small Board)**

**USB3.0 (TYPE C)**

## HDA Bus(CLG)





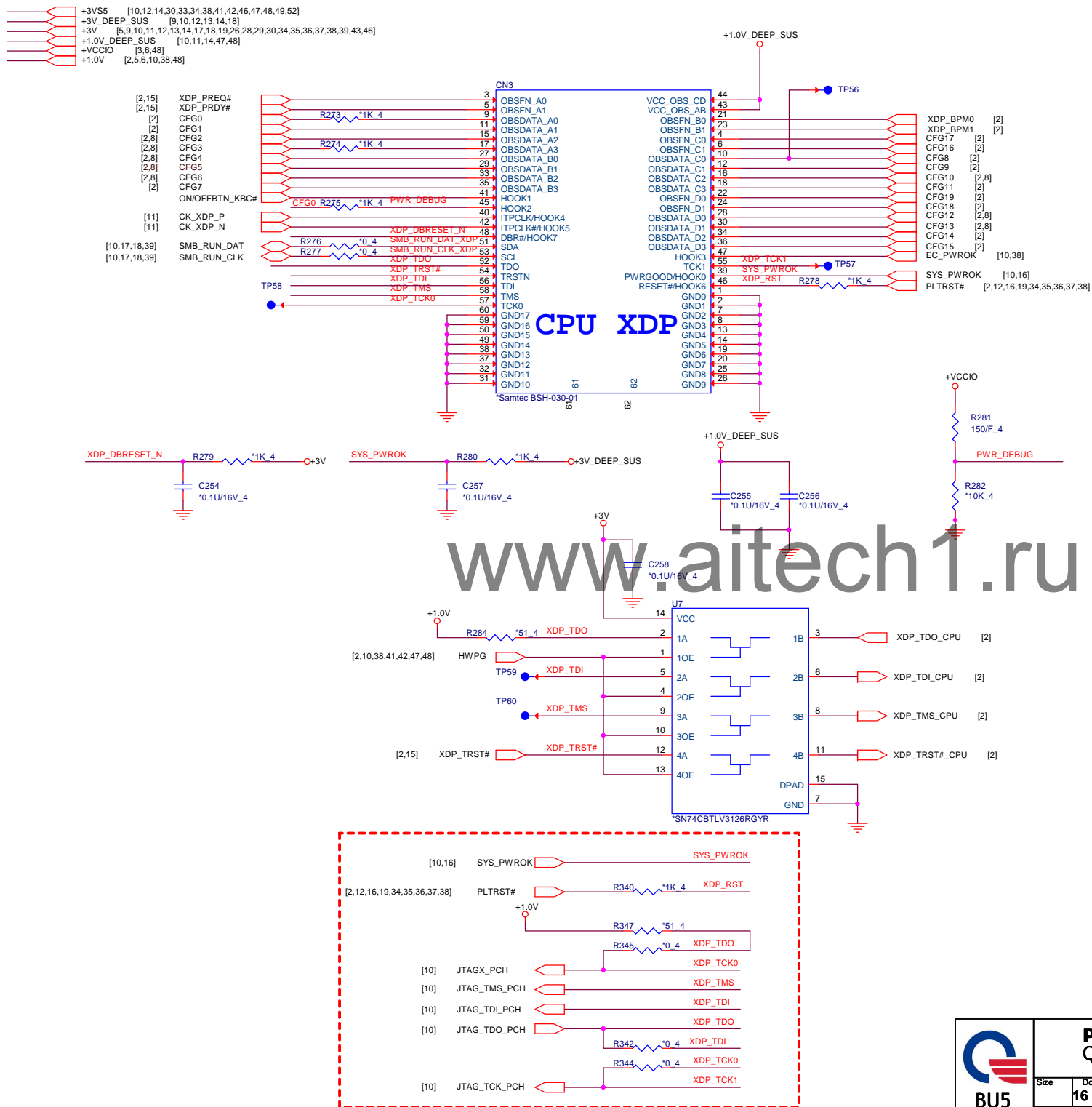








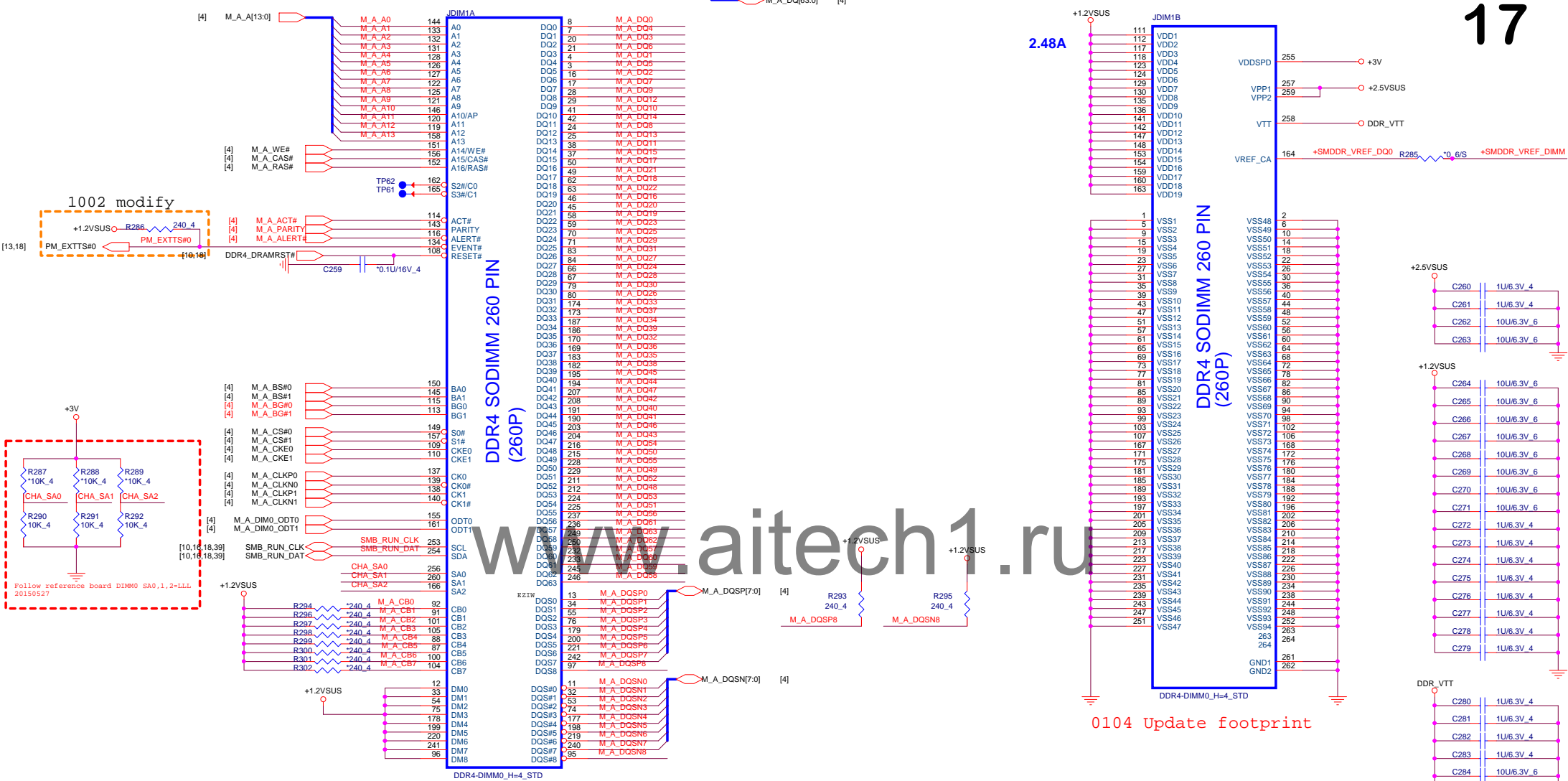




**PROJECT : G75C**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>16 -- XDP &amp; APS</b>	1A
Date: Monday, December 05, 2016	Sheet 16 of 52	



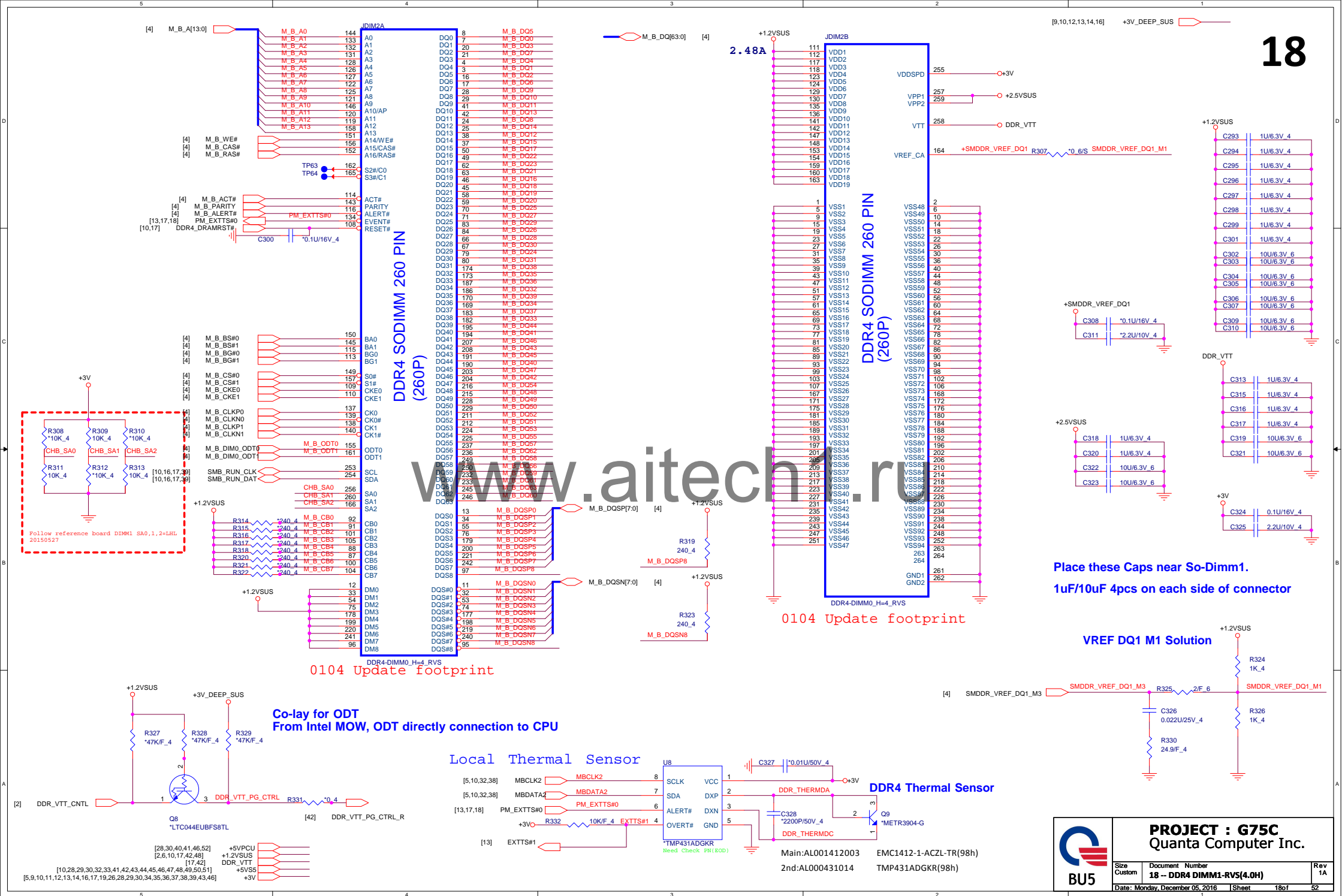


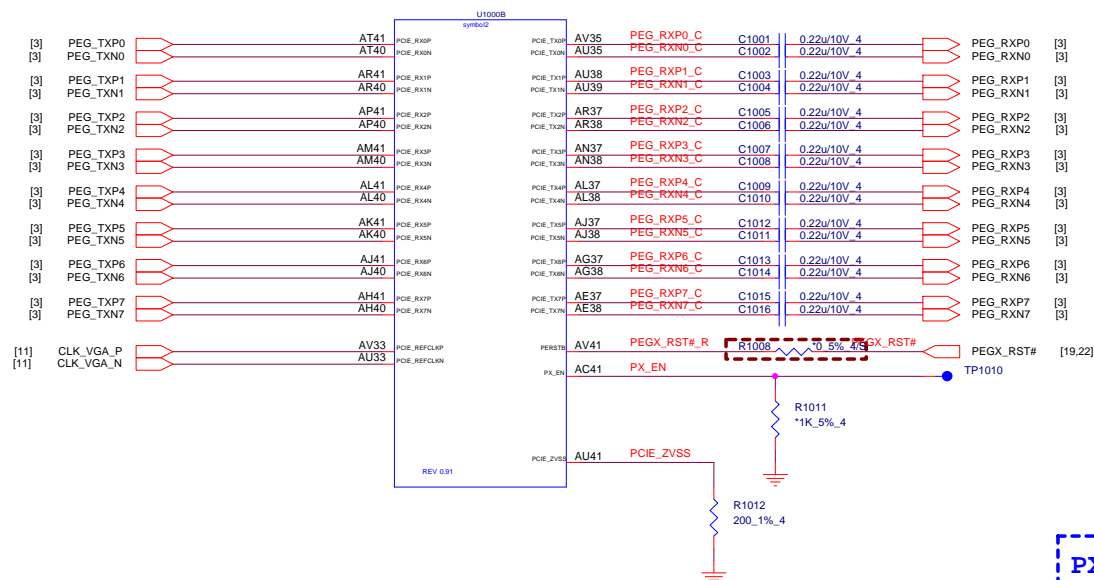
0104 Update footprint

Place these Caps near So-Dimm0.

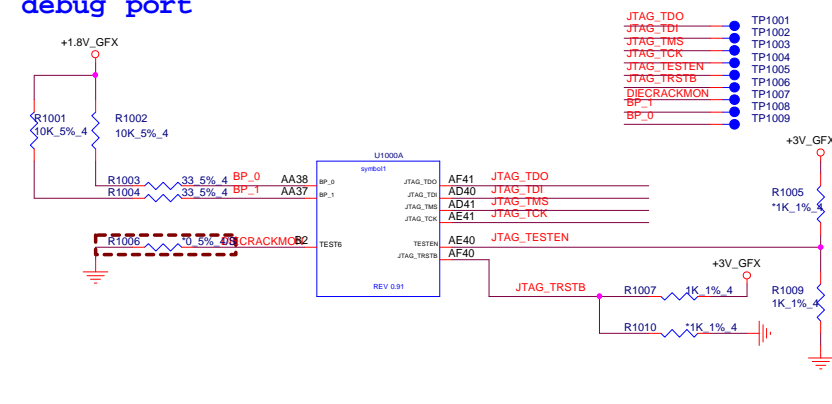
1uF/10uF 4pcs on each side of connector

+1.2VSUS [2,6,10,18,42,48]  
+3V [5,9,10,11,12,13,14,16,18,19,26,28,29,30,34,35,36,37,38,39,43,46]

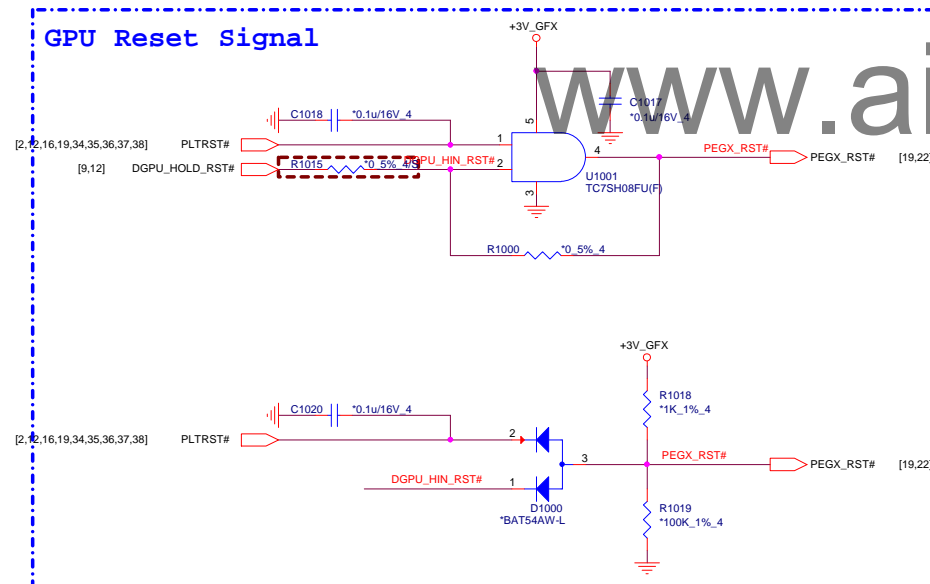




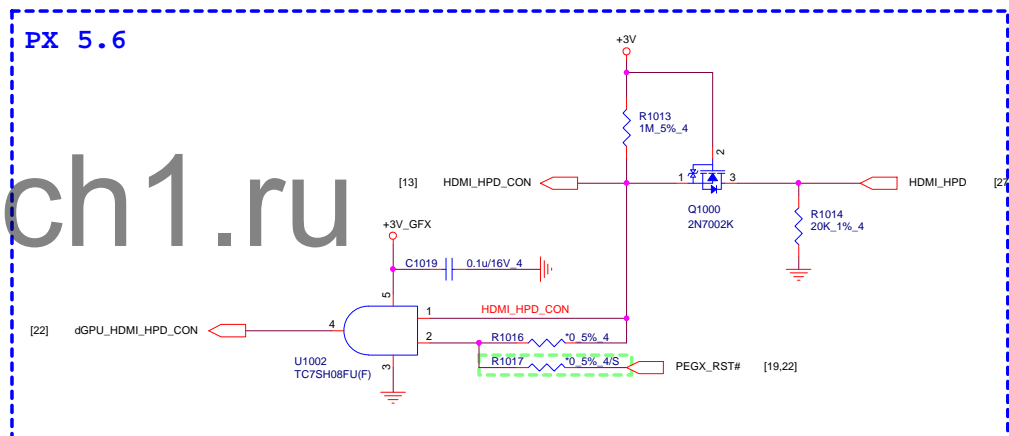
## debug port



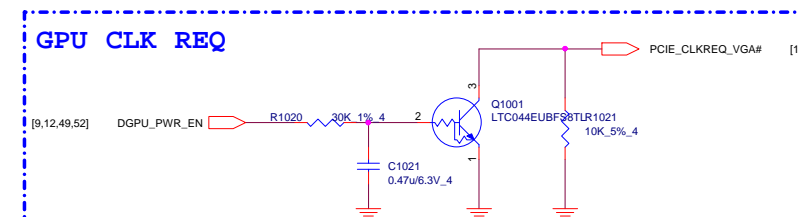
## GPU Reset Signal



## PX 5.6

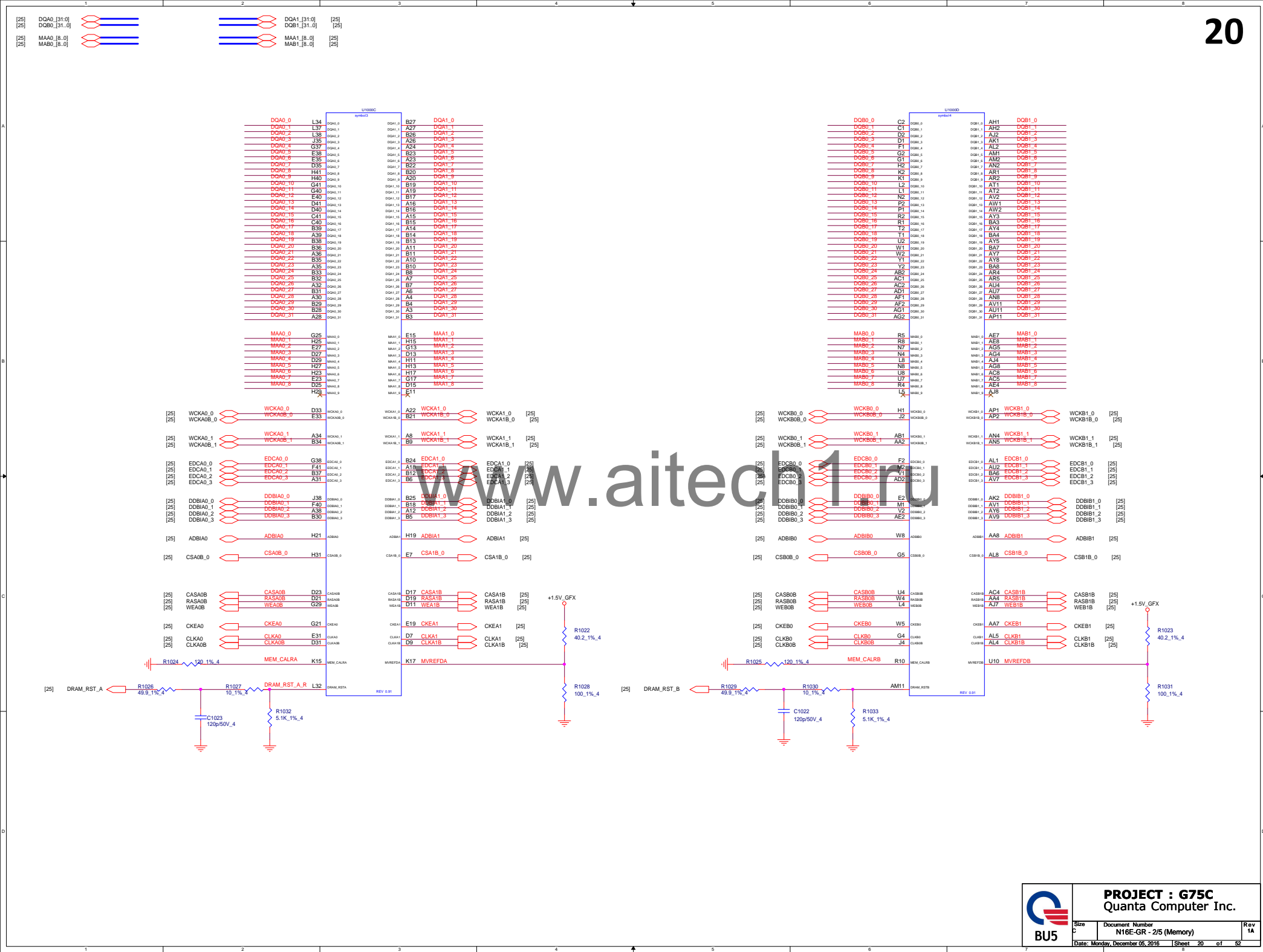


## GPU CLK REQ



**PROJECT : G75C**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16P-GX/GT - 1/5 (PCIE)	1A
Date: Tuesday, March 07, 2017	Sheet 19 of 52	



ASIC - TMDP (A/B)

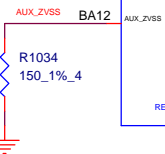
U1000G

symbol7

TX2P\_DP0P AY32  
 TX2M\_DP0N BA32  
 TX1P\_DP0P AY31  
 TX1M\_DP0N BA31  
 TX0P\_DP0P AY30  
 TX0M\_DP0N BA30  
 TXCBP\_DP0P AY28  
 TXCBM\_DP0N BA28

DDCAUXP AM21  
 DDCAUXN AP21

TX2P\_DP0P AY36  
 TX2M\_DP0N BA36  
 TX1P\_DP0P AY35  
 TX1M\_DP0N BA35  
 TX0P\_DP0P AY34  
 TX0M\_DP0N BA34  
 TXCBP\_DP0P AY33  
 TXCBM\_DP0N BA33



AUX\_ZVSS

BA12

AUX\_ZVSS

REV 0.91

DDCAUXP AR23 GPU\_DDCCLK [27]  
 DDCAUXN AP23 GPU\_DDCDATA [27]

ASIC - TMDP (C/D)

U1000H

symbol8

TX2P\_DP0P AY22  
 TX2M\_DP0N BA22  
 TX1P\_DP0P AY21  
 TX1M\_DP0N BA21  
 TX0P\_DP0P AY20  
 TX0M\_DP0N BA20  
 TXCBP\_DP0P AY19  
 TXCBM\_DP0N BA19

AUX1P AY11  
 AUX1N BA11

DDCCLK AY10 TP1000  
 DDCDATA BA10 TP1011

TX2P\_DP0P AY27  
 TX2M\_DP0N BA27  
 TX1P\_DP0P AY26  
 TX1M\_DP0N BA26  
 TX0P\_DP0P AY25  
 TX0M\_DP0N BA25  
 TXCBP\_DP0P AY24  
 TXCBM\_DP0N BA24

AUX2P AP19  
 AUX2N AM19

DDCCLK AV19  
 DDCDATA AU19

REV 0.91

GPU\_D2 [27]  
 GPU\_D2# [27]  
 GPU\_D1 [27]  
 GPU\_D1# [27]  
 GPU\_D0 [27]  
 GPU\_D0# [27]  
 GPU\_CLK [27]  
 GPU\_CLK# [27]

ASIC - TMDP (E)

U1000O

symbol15

TX2P\_DP0P AY18  
 TX2M\_DP0N BA18  
 TX1P\_DP0P AY16  
 TX1M\_DP0N BA16  
 TX0P\_DP0P AY15  
 TX0M\_DP0N BA15  
 TXCBP\_DP0P AY14  
 TXCBM\_DP0N BA14

DDCAUXP AU27  
 DDCAUXN AV27

REV 0.91

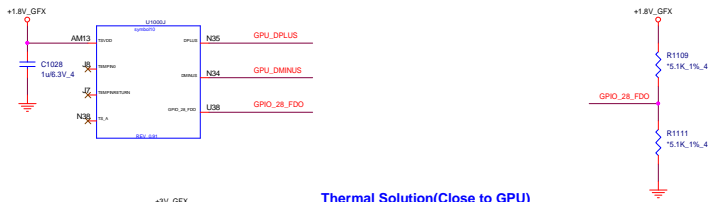


**PROJECT : G75C**  
 Quanta Computer Inc.

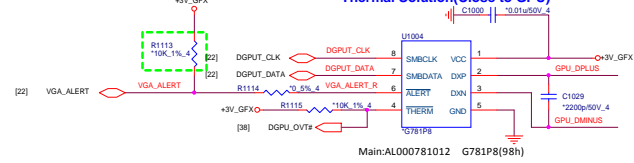
Size	Document Number	Rev
B	N16E-GR - 3/5 (Display)	1A
Date: Monday, December 05, 2016	Sheet 21 of 52	



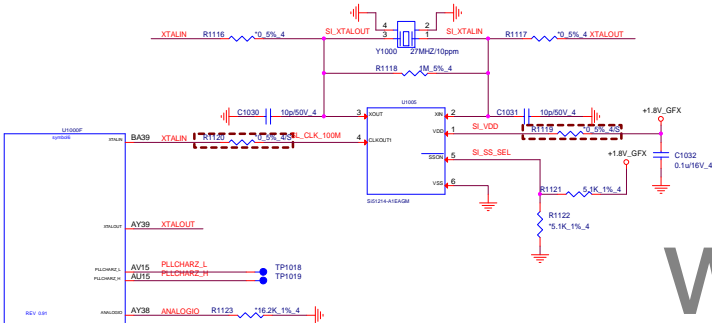
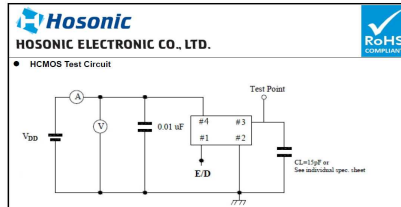




Thermal Solution(Close to GPU)



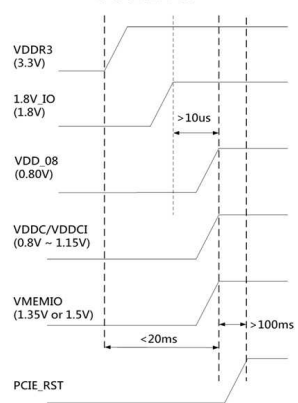
Main:AL000781012 G781P8(98h)



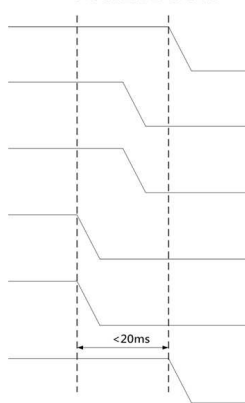
www.aitech1.ru

B10M-G1-10 Power up sequence for you refer:

## POWER UP



## POWER DOWN

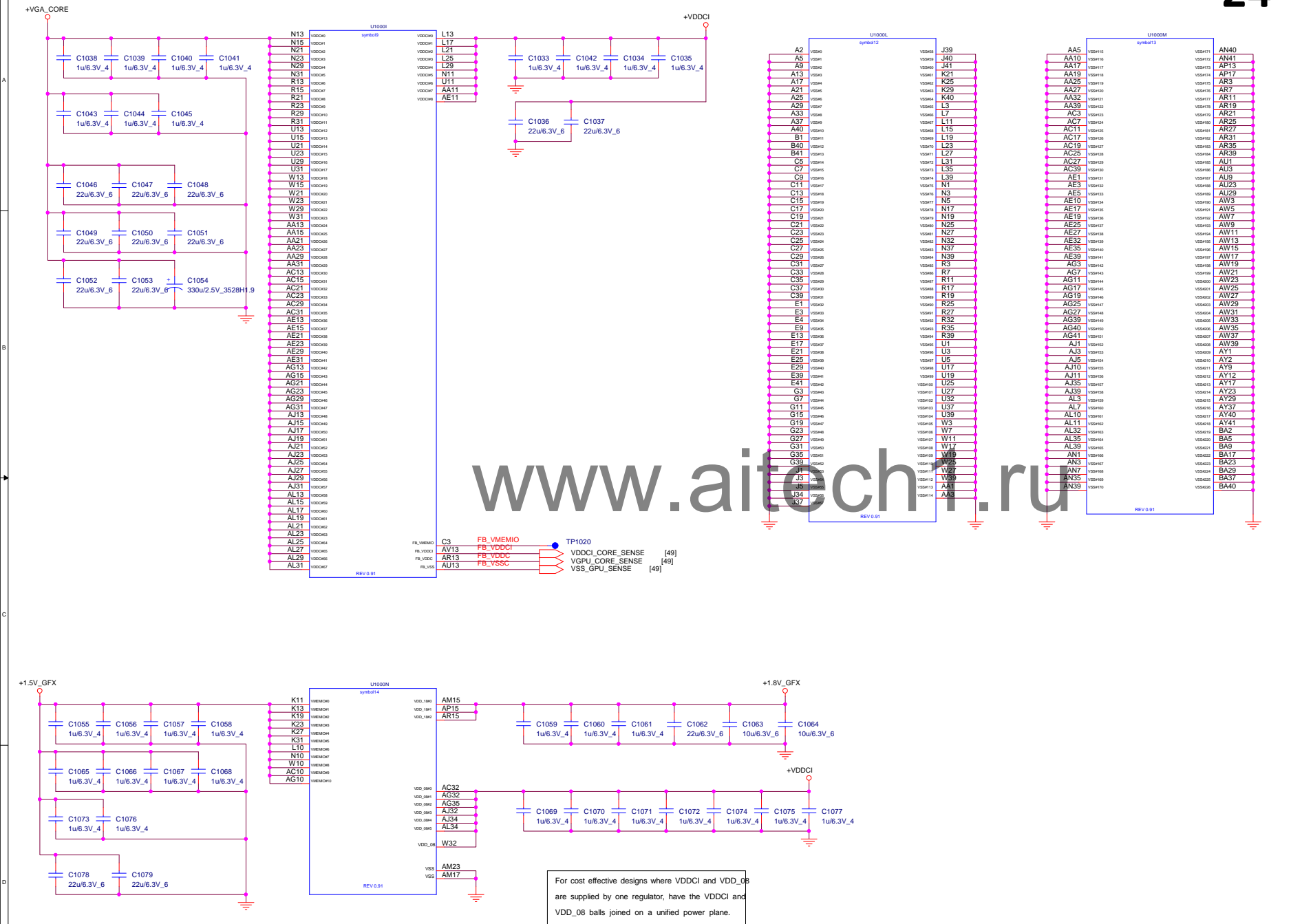


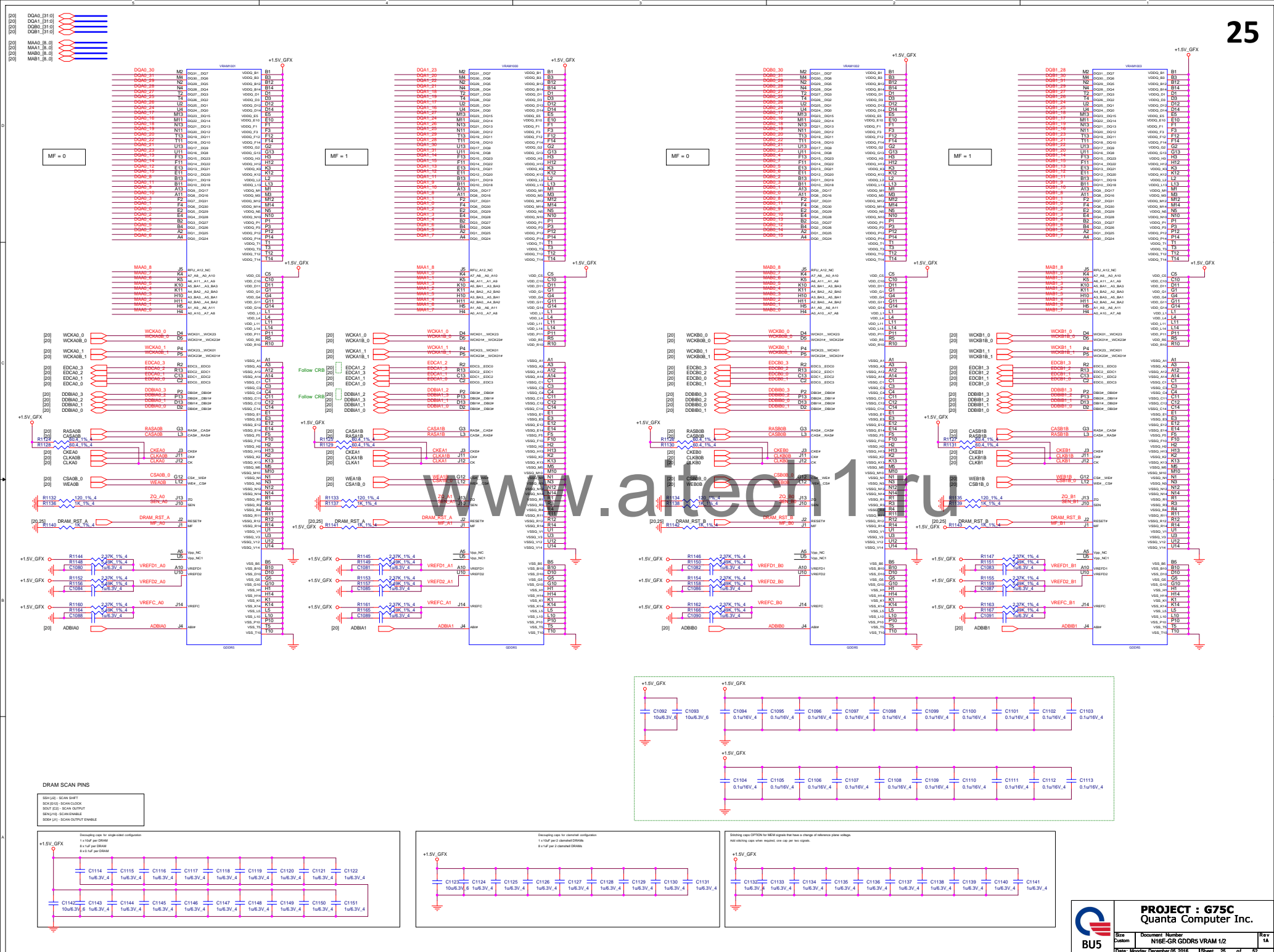
AMD GPIO Strapping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 1K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) if BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_[13:12:11]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hsync	NC	Reserve	Reserve
Vsync	NC	Reserve	Reserve
DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVDD[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		



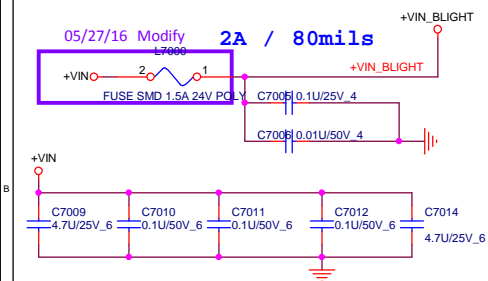
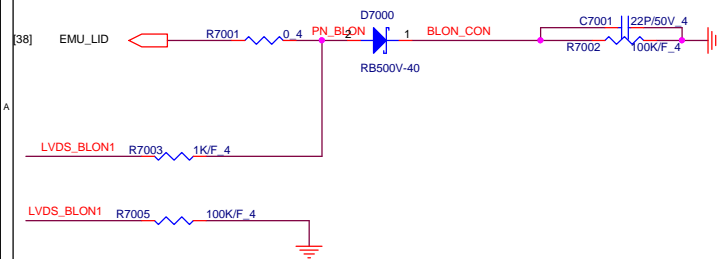
**PROJECT : G75C**  
Quanta Computer Inc.

Size: Custom  
Document Number: N16P-GXGT - 2/5 (Memory)  
Date: Friday, January 06, 2017 Sheet: 23 of 52 Rev: 1A

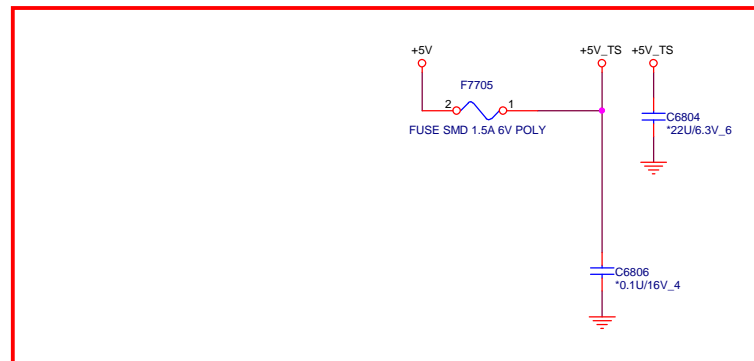
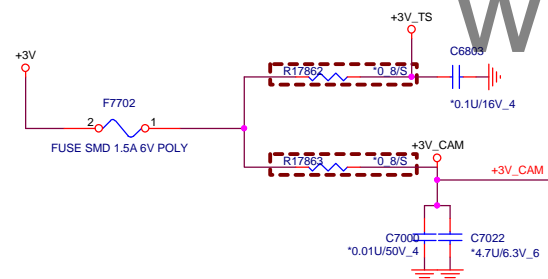




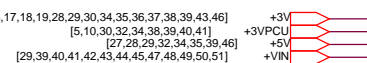
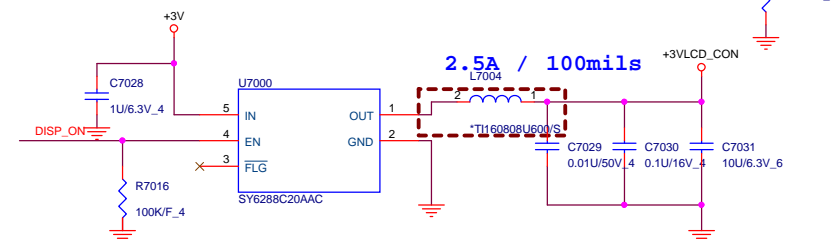
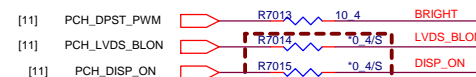
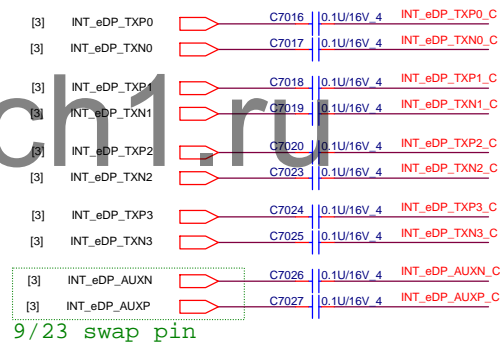
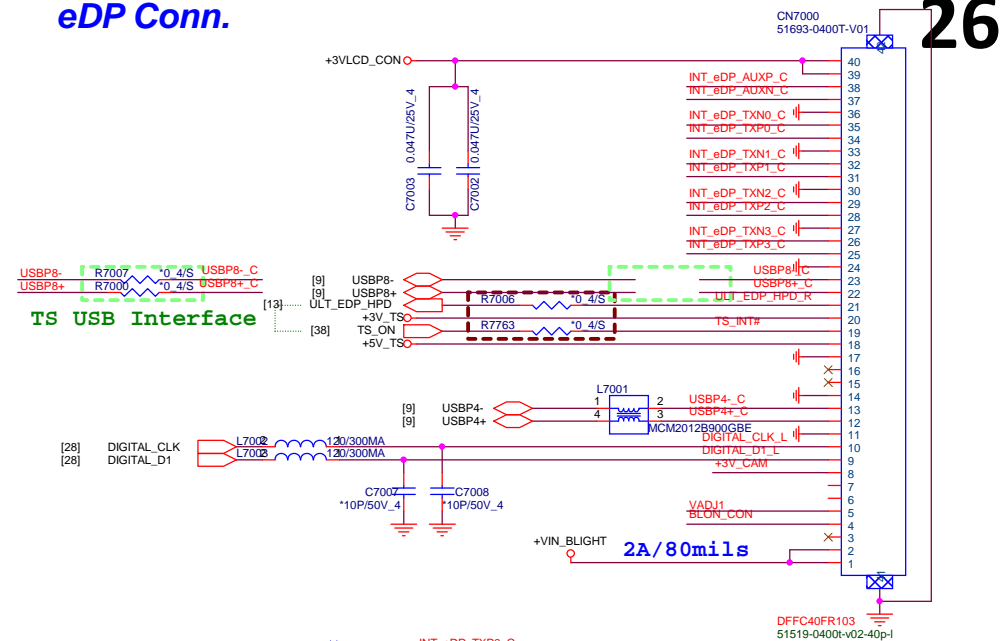
## LID Switch



## Touch screen



**eDP Conn.**



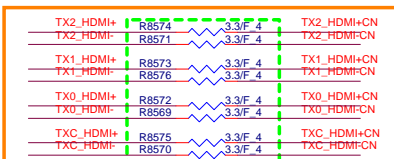
[5,9,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,37,38,39,43,46]

+3V

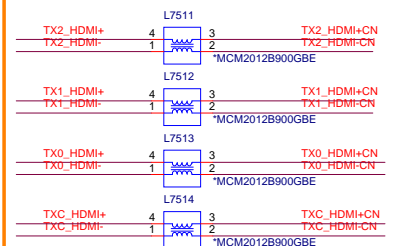
[26,28,29,32,34,35,39,46]

+5V

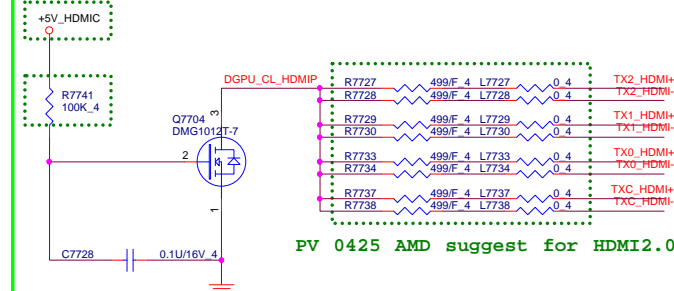
## EMI Solution DB 0126 modify



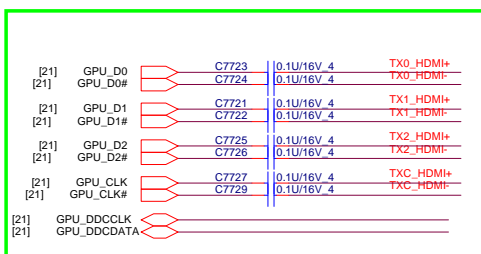
SI 1205 AMD suggest mount 3.3R



## DB 0118 Change to +5V\_HDMIC



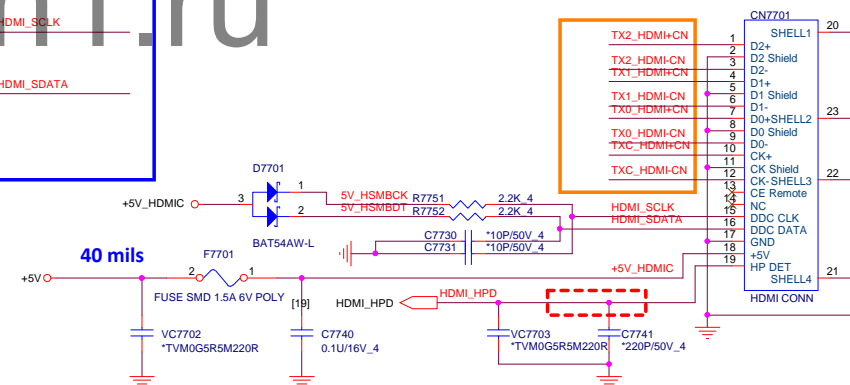
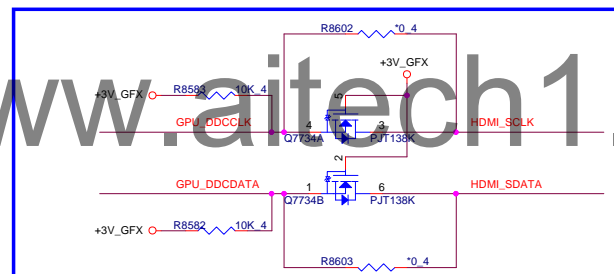
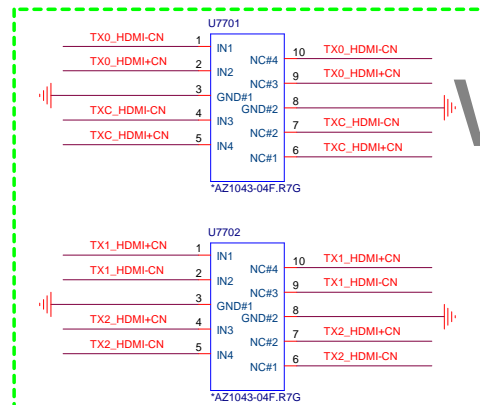
PV 0425 AMD suggest for HDMI2.0



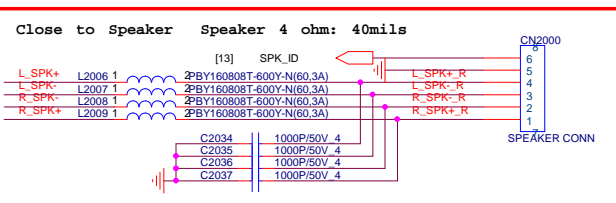
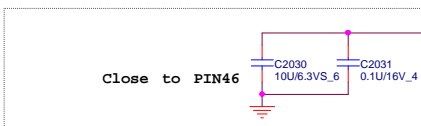
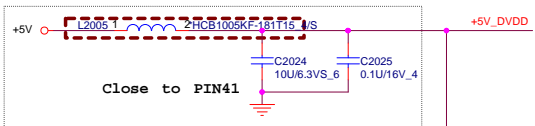
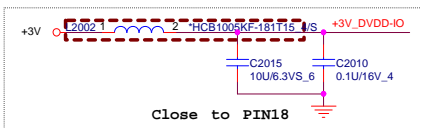
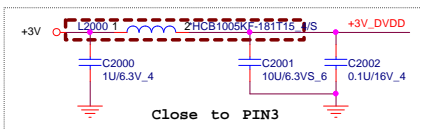
## HDMI SMBus Isolati on

Close to HDMI connector

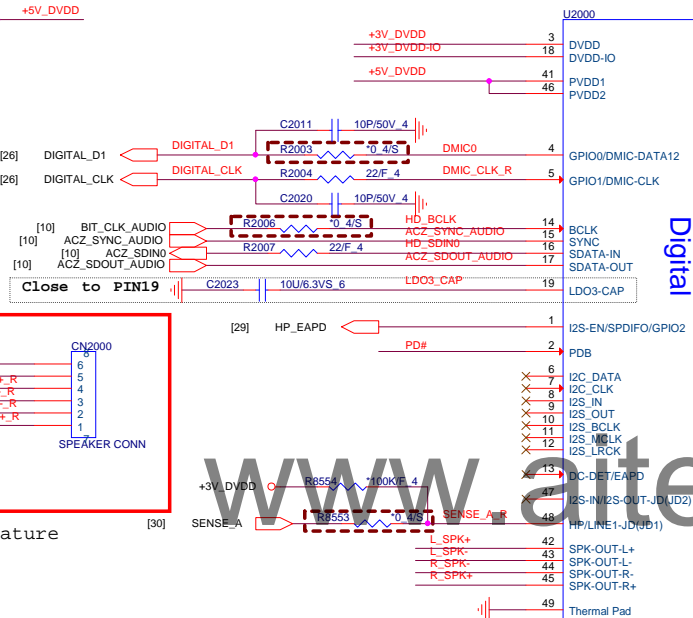
## ESD



SI 0310 AMD suggest not mount



1124 Add SPK\_ID for Smart amp feature



Digital

Analog

ALC3258-CG x QFN48

AVDD1

CPVDD/AVDD2

AVSS2

AVSS1

LDO1-CAP

LDO2-CAP

VREF

CBP

CBN

CPVEE

MIC2-CAP

LINE1-L(PORT-C-L)

LINE1-R(PORT-C-R)

PCBEEP

5VSTB/AUX MODE

MIC2-R/SLEEVE

MIC2-L/RINSE

MIC2-VREFOUT

MIC2-VREFOUT-L

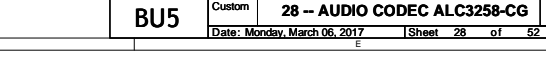
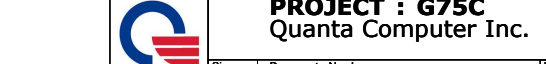
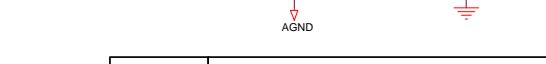
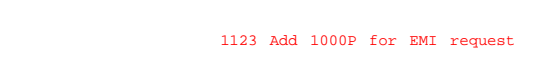
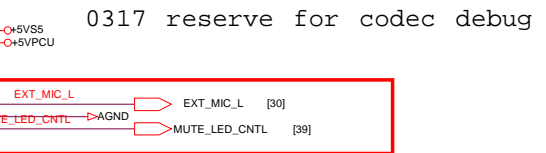
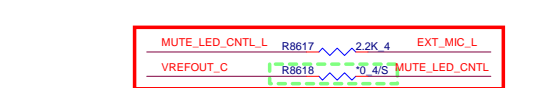
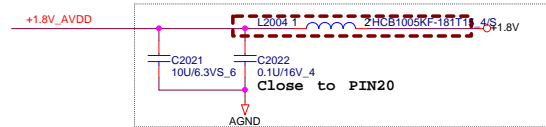
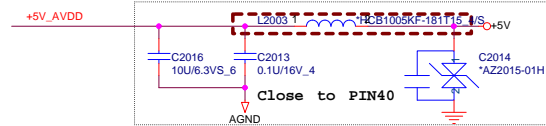
MIC2-VREFOUT-R

HPOUT-L(PORT-I-L)

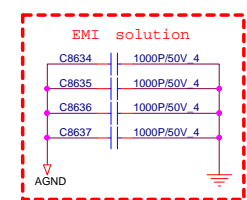
HPOUT-R(PORT-I-R)

AGND SHIELD

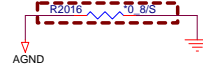
+5V\_AVDD >40mils trace



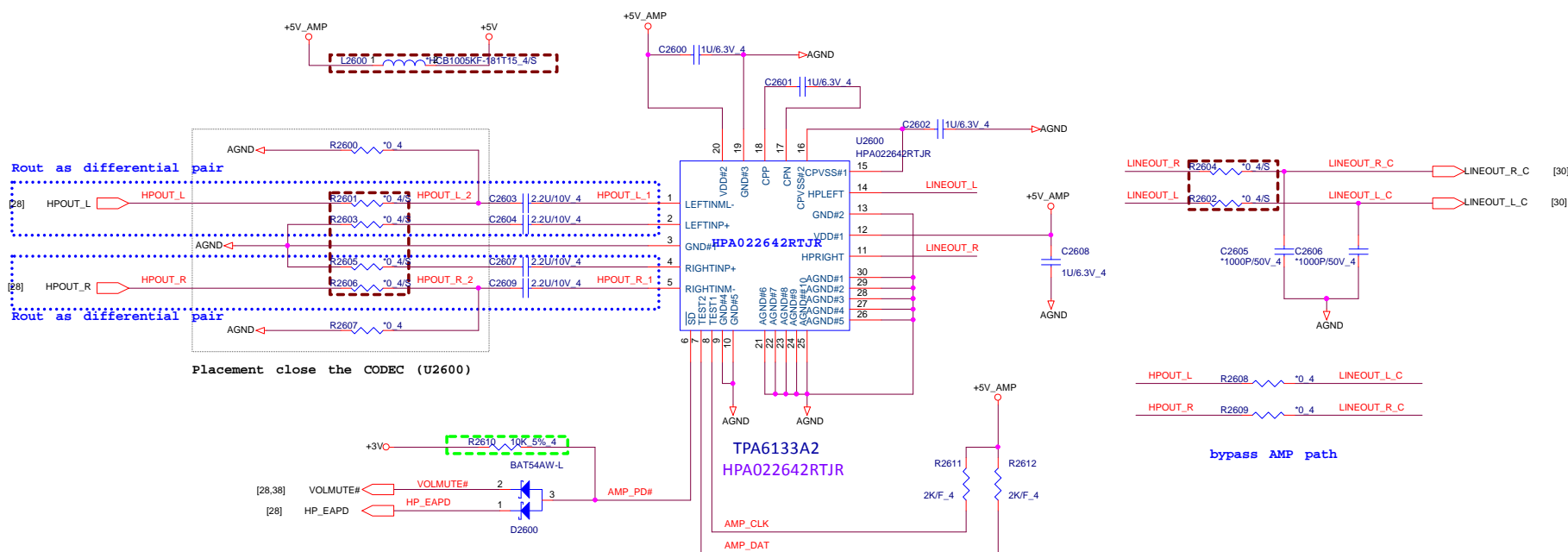
1123 Add 1000P for EMI request



place to near or under codec

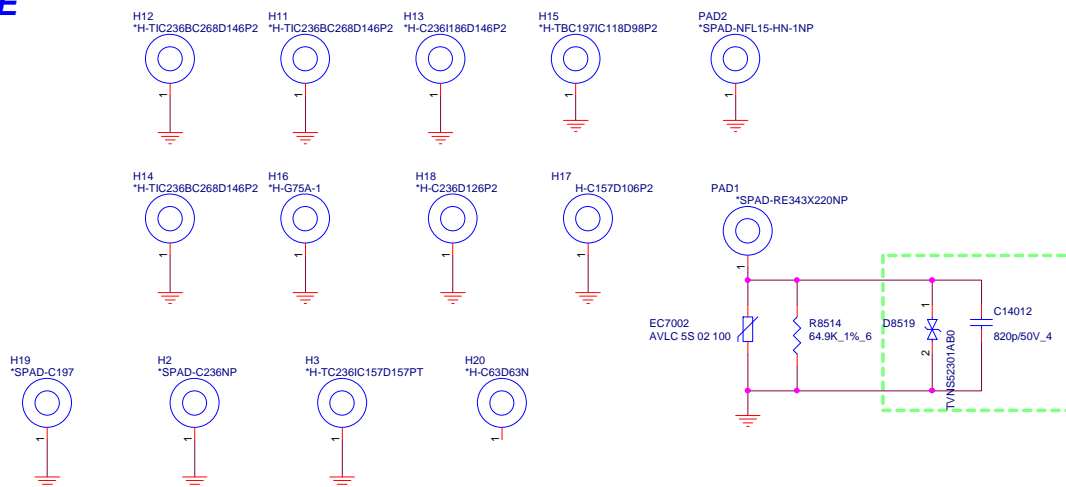




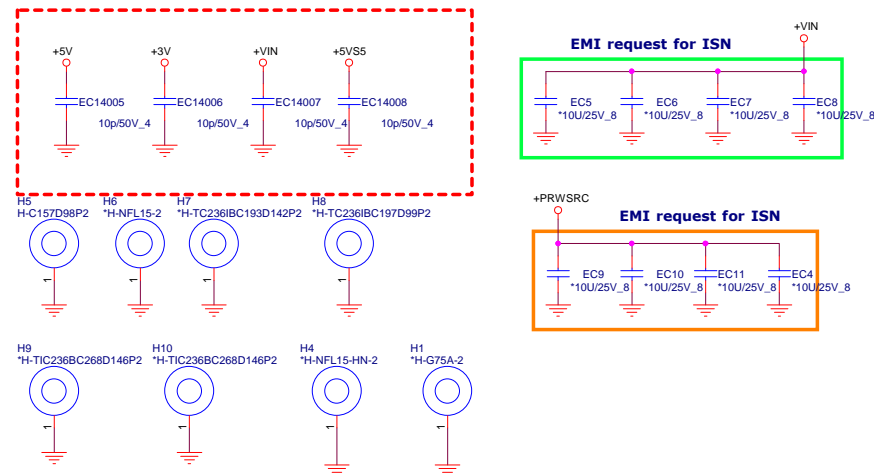


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## HOLE




## RF





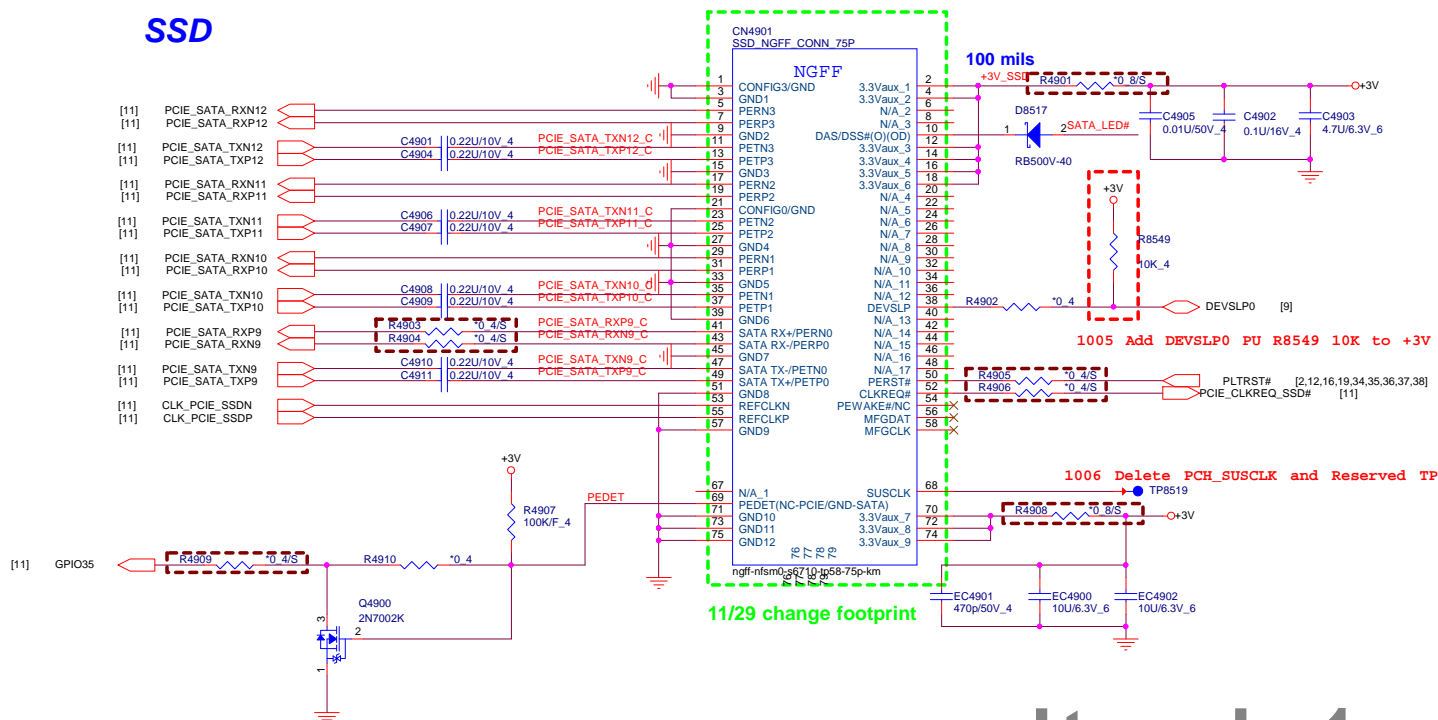
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 BU5	<b>PROJECT : G75C</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>RF Solution</b>	Rev 1A
	Date: Monday, December 05, 2016    Sheet 31 of 52		

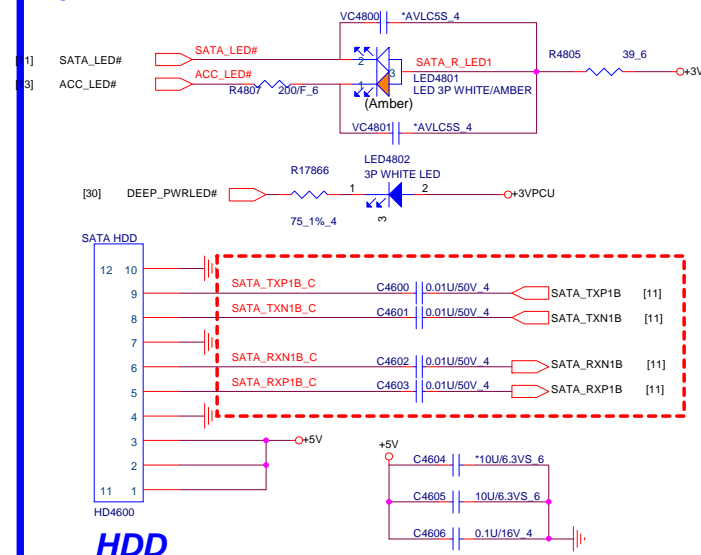


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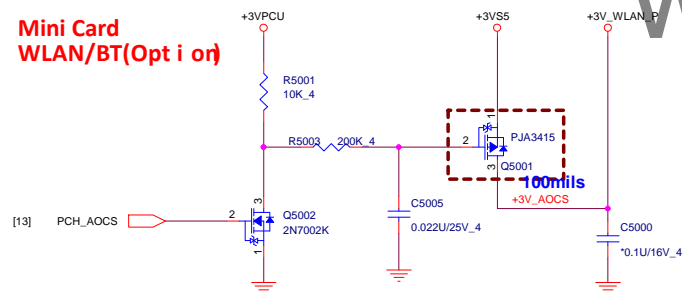
## SSD



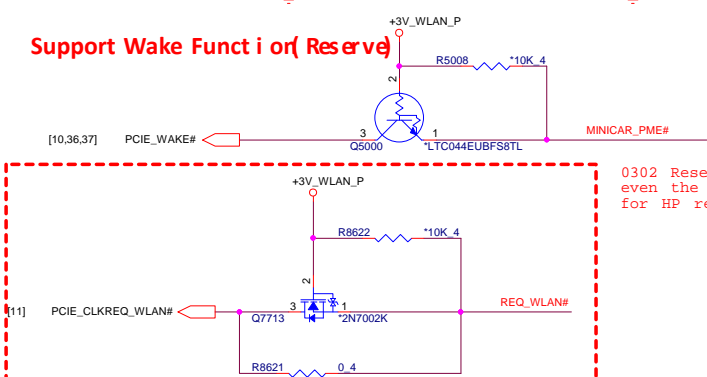
**SATA LED**

**HDD**

**Mini Card  
WLAN/BT(Optional)**

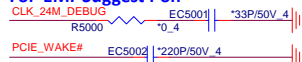


### Support Wake Function( Reserve)

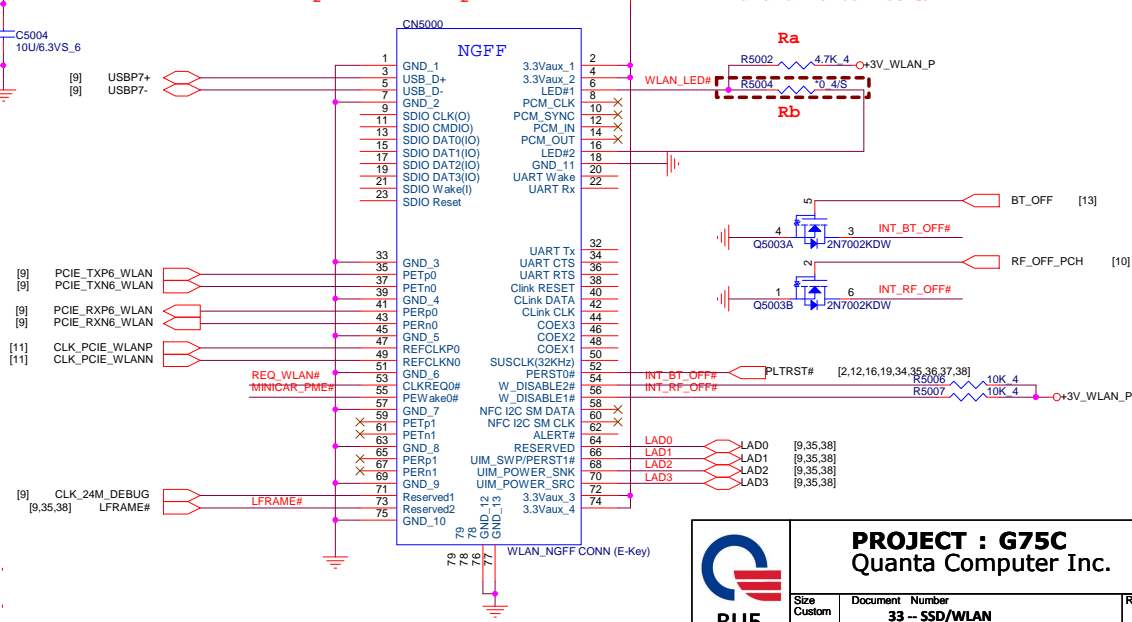


```
0302 Reserved the MOSFET at CLKREQ#
even the current leakage test passed
for HP requested
```

For EMI Suggest i on



1225 Update footprint



Remove Net RF\_LINK# and need check if  
Ra and Rb can be NI

**PROJECT : G75C**  
Quanta Computer Inc.



BU5

Size	Document Number
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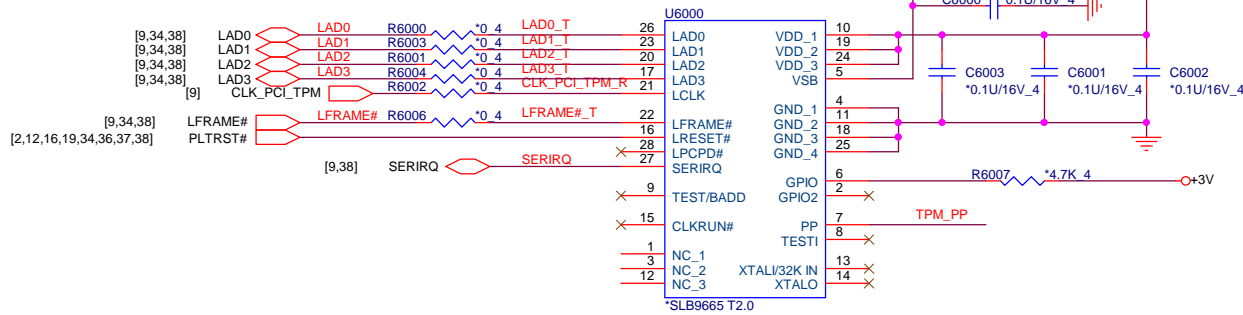
Custom 33 -- SSD/WLAN

Rev	
-----	--

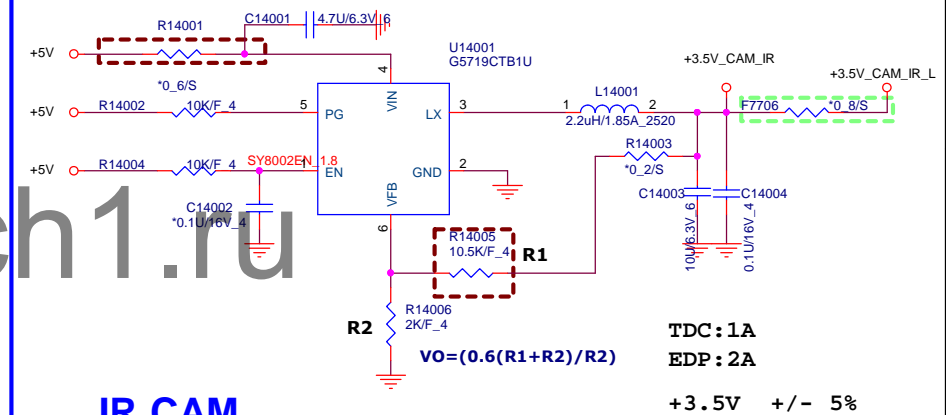
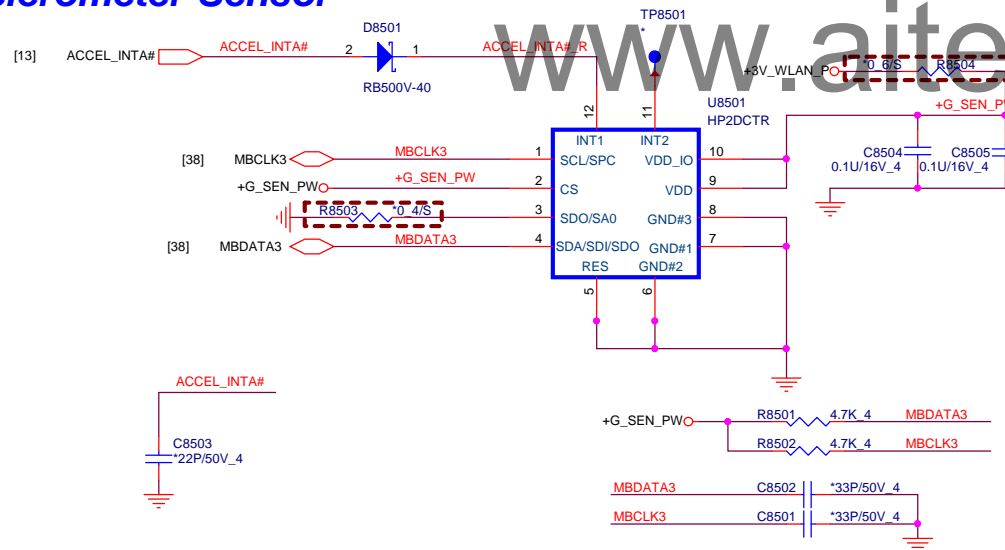


## TPM (2.0)

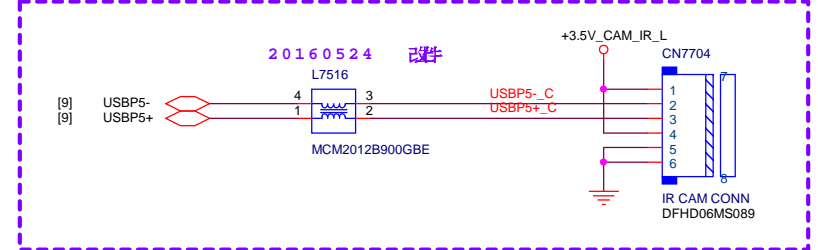
PN:AL009665K01



## Accelerometer Sensor



## IR CAM



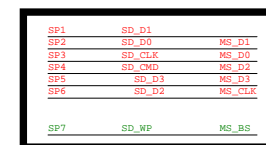
**PROJECT : G75C**  
**Quanta Computer Inc.**

Size	Document Number	Rev
B	34 - TPM/G-Sensor	1A
Date: Monday, March 06, 2017	Sheet 35 of 52	

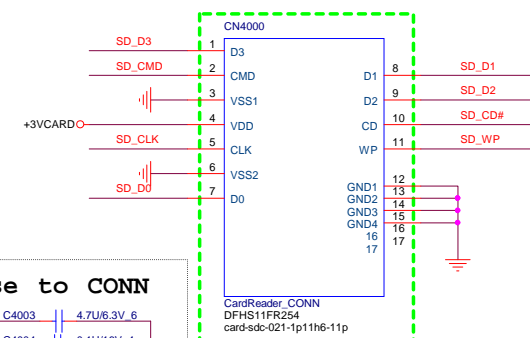
## LAN & RJ45

<b>PROJECT : G75C</b> <b>Quanta Computer Inc.</b>		
Size Custom	Document Number <b>35 – LAN RTL8107ESH-CG/RJ45</b>	Rev 1A
Date: Monday, March 06, 2017	Sheet 36 of 52	

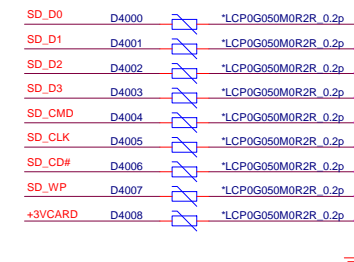
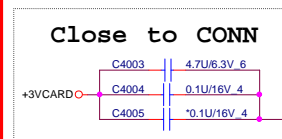
+3V

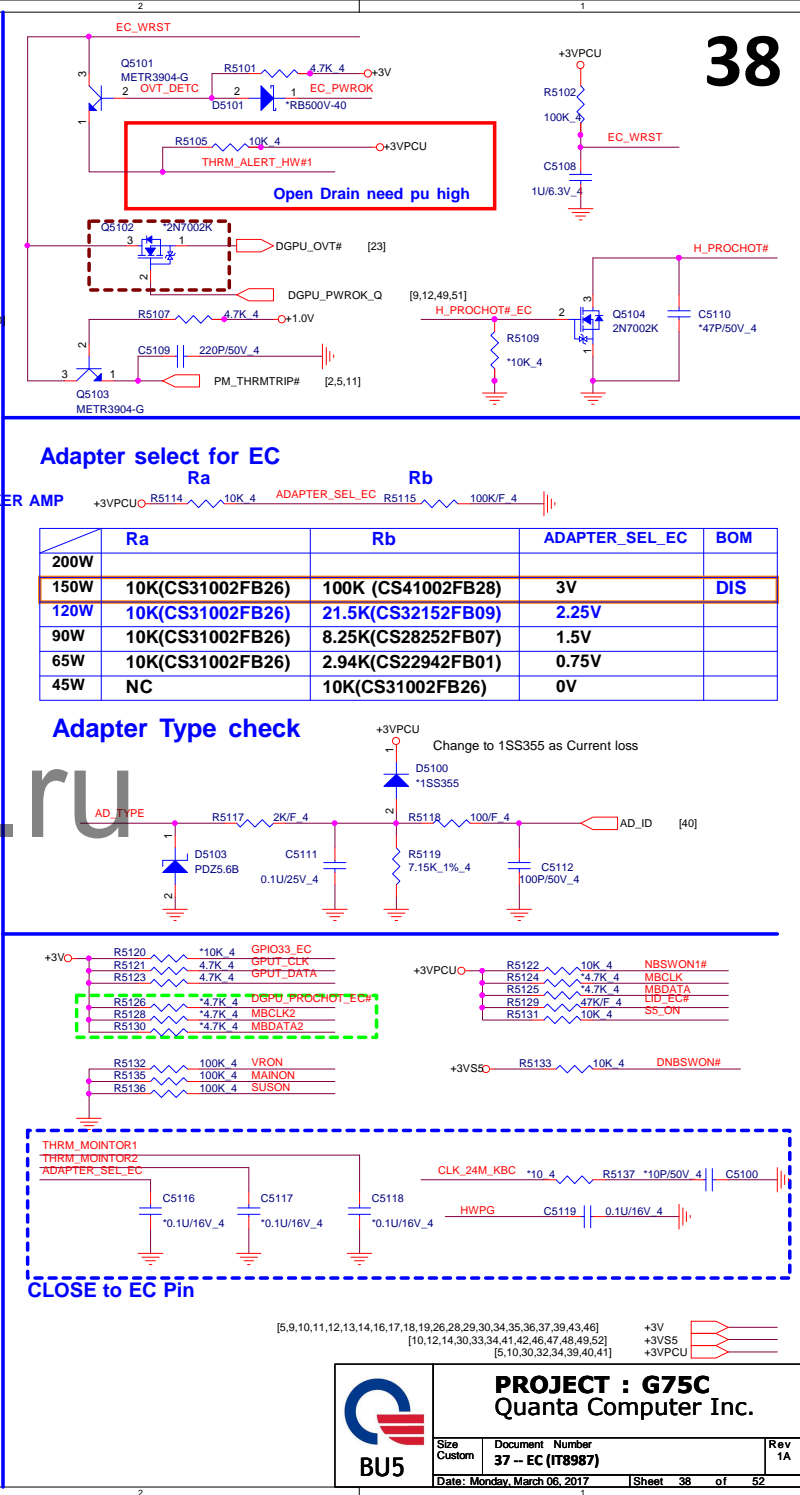


SD / MMC

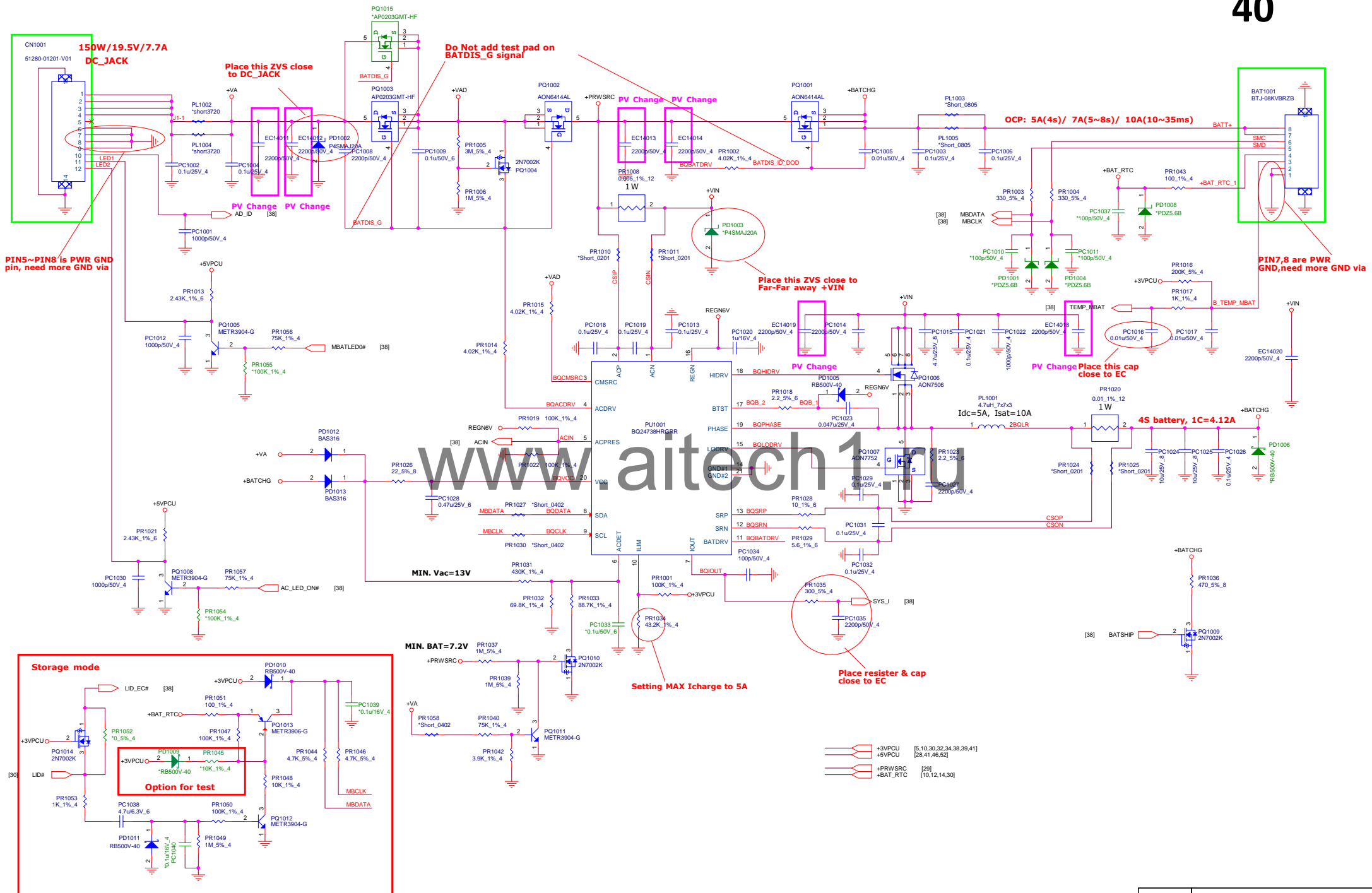


- 12/02 change footprint & pin define

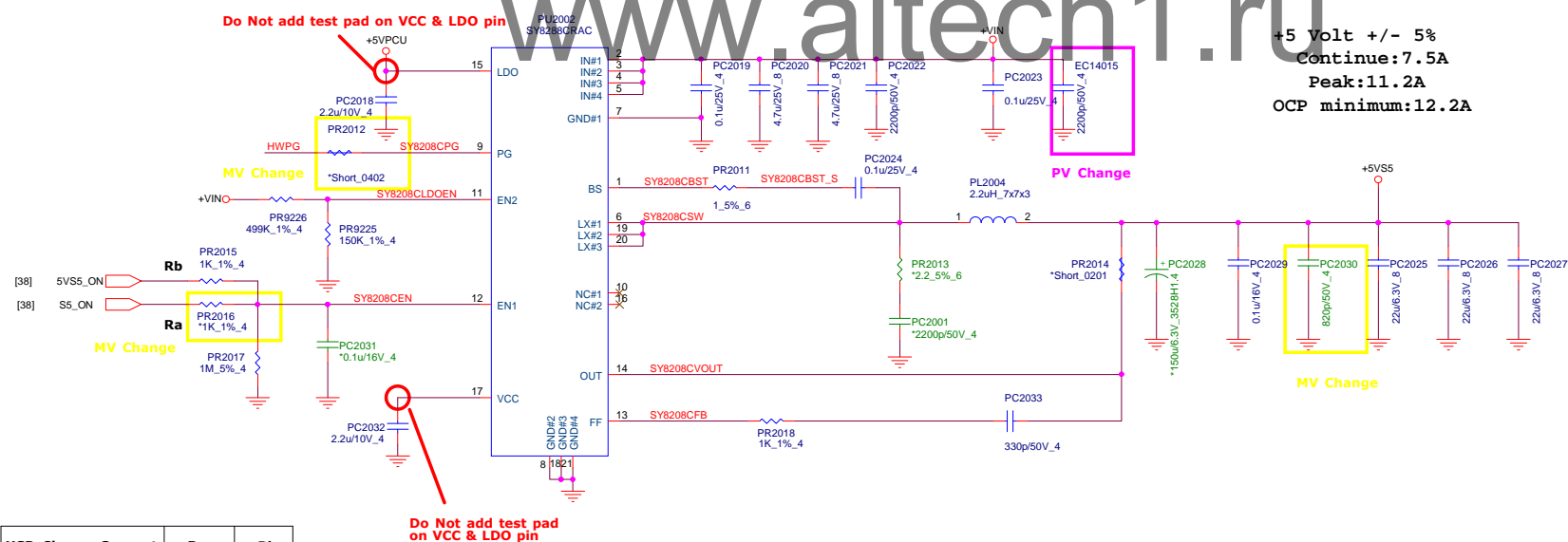
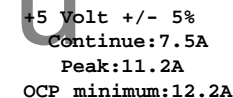
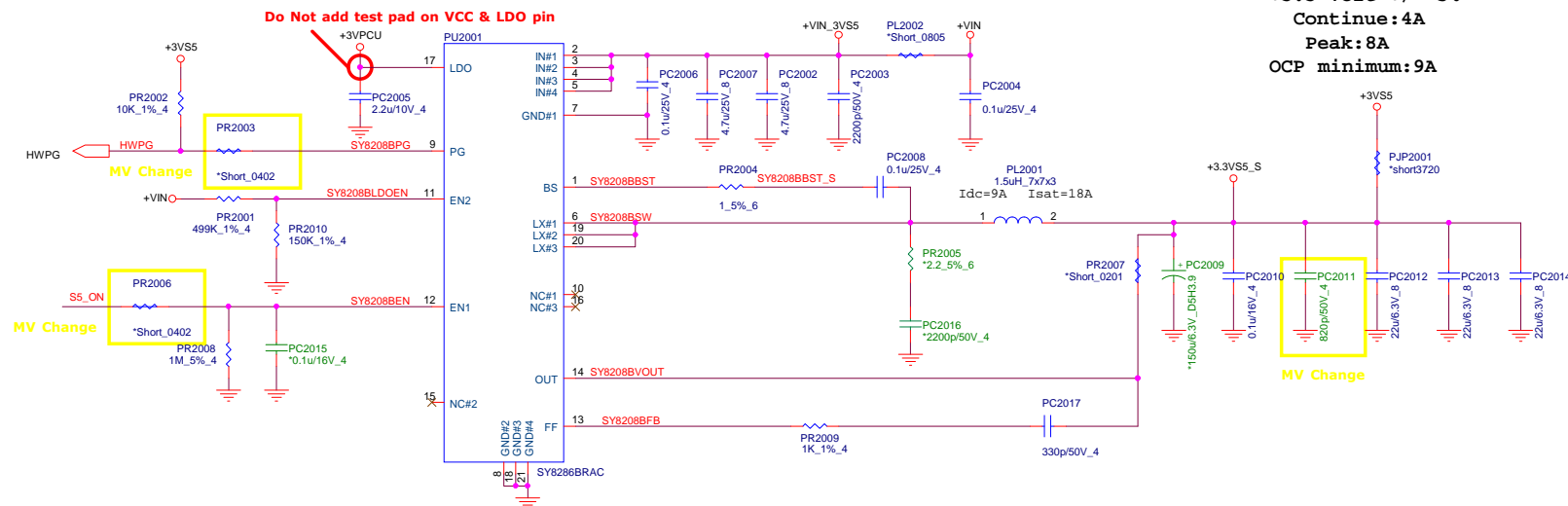
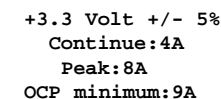




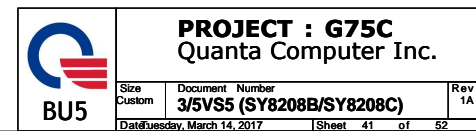
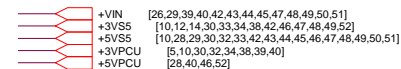


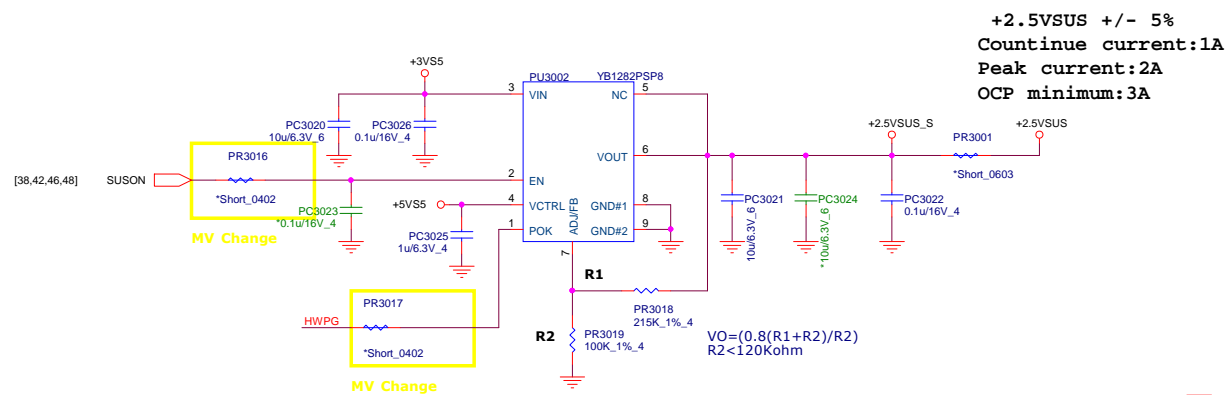
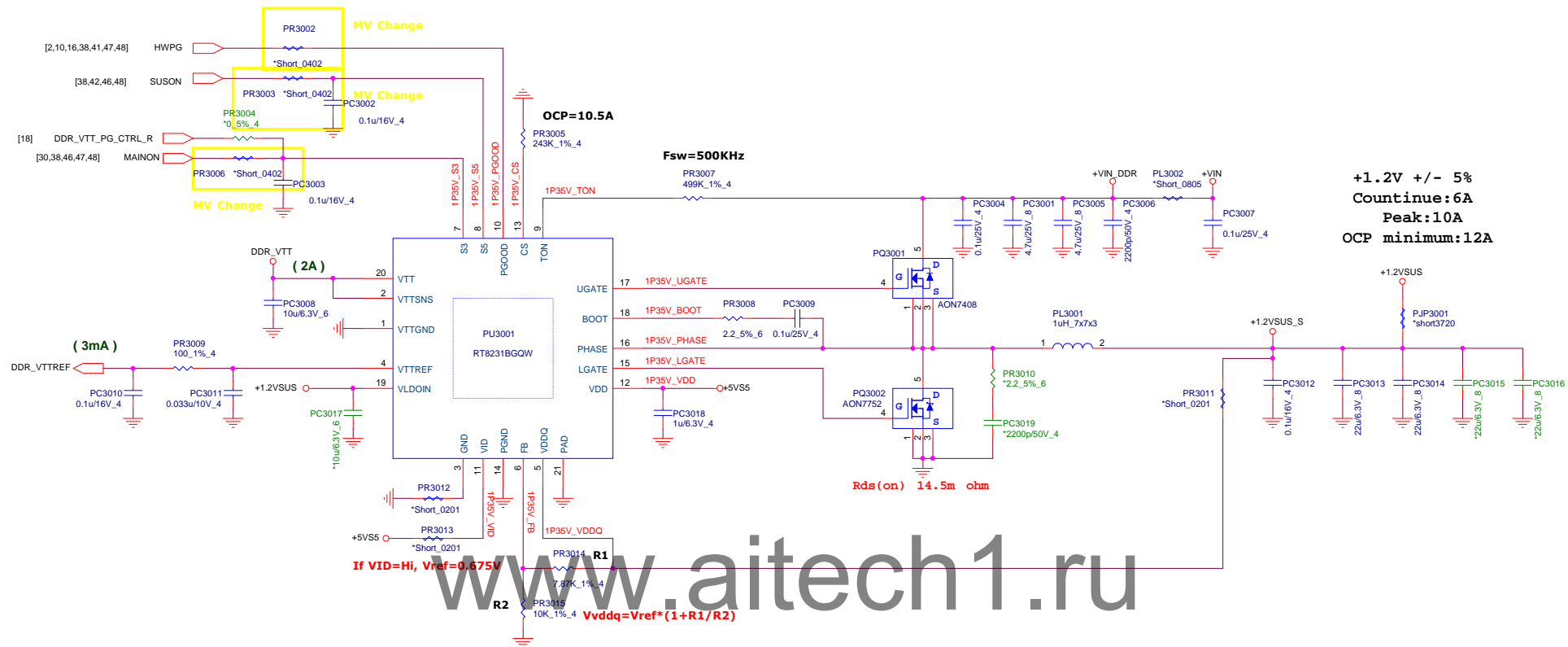







USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

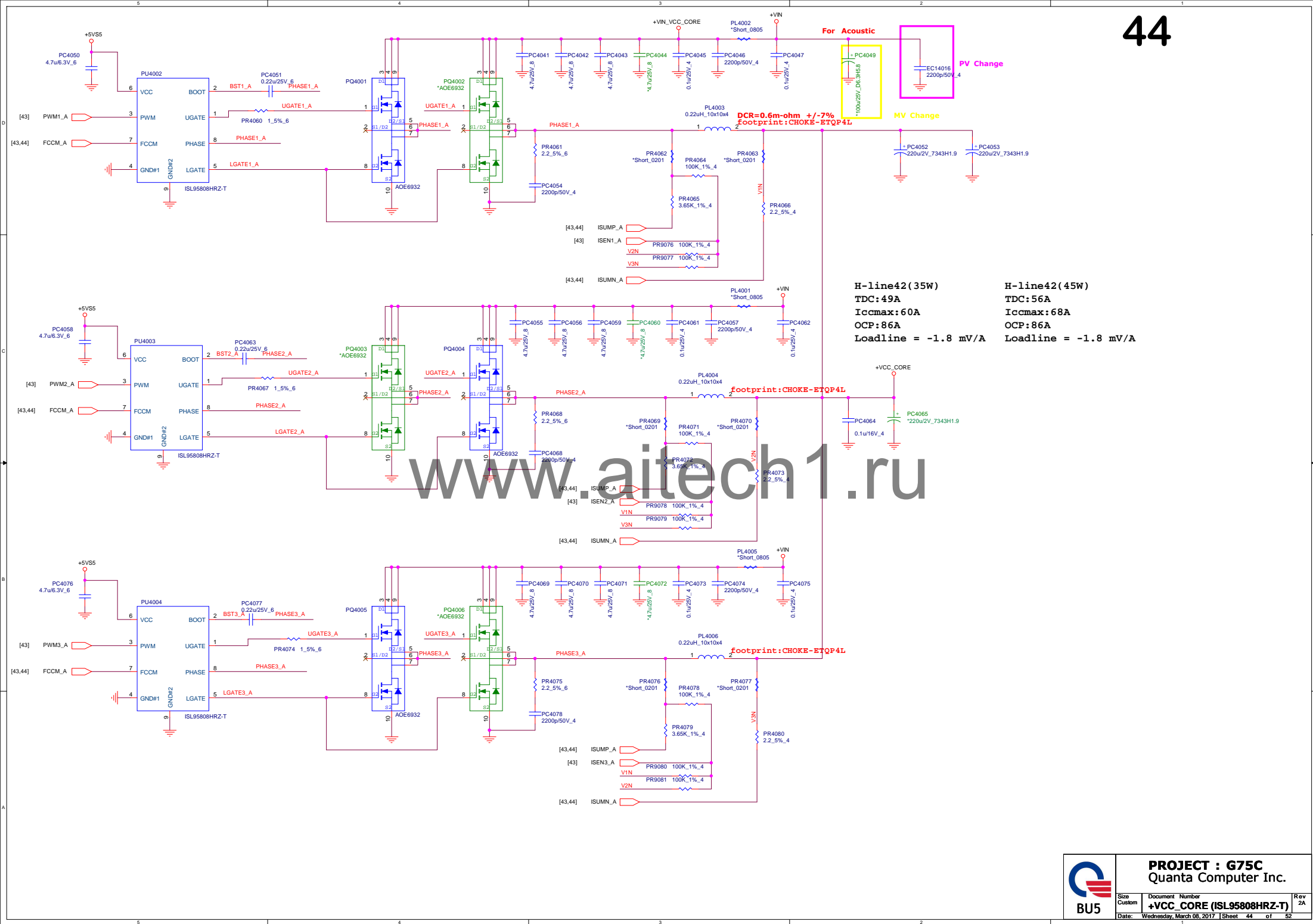




+VIN	[26,29,39,40,41,43,44,45,47,48,49,50,51]
+5VS5	[10,28,29,30,32,33,41,43,44,45,46,47,48,49,50,51]
+1.2VSUS	[2,6,10,17,18,48]
DDR_VTT	[17,18]
+2.5VSUS	[17,18]

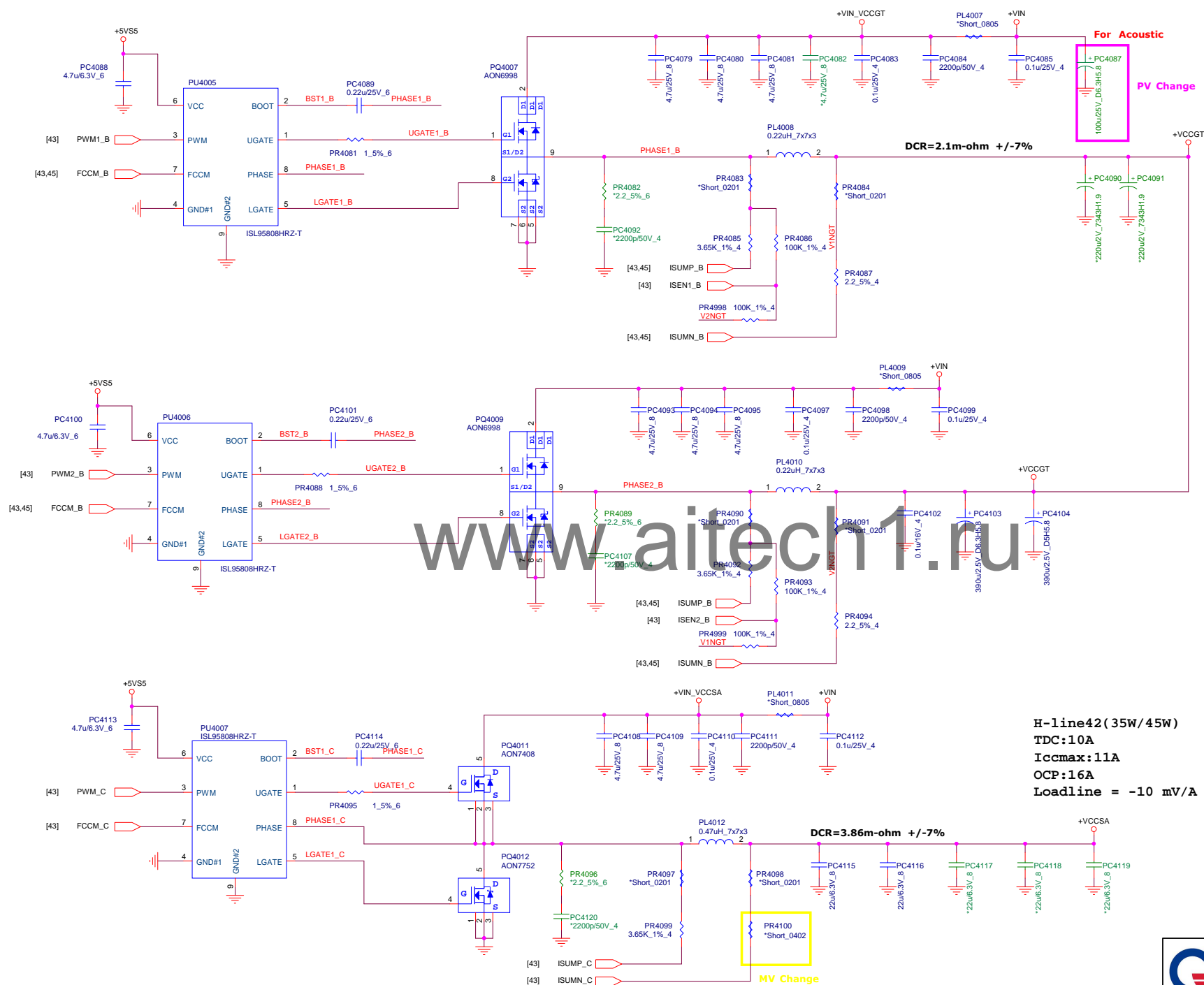
			<b>PROJECT : G75C</b> Quanta Computer Inc.	
Size	Document Number		Rev	
	BU5		1A	
Wednesday, March 08, 2017			Sheet 42 of 52	





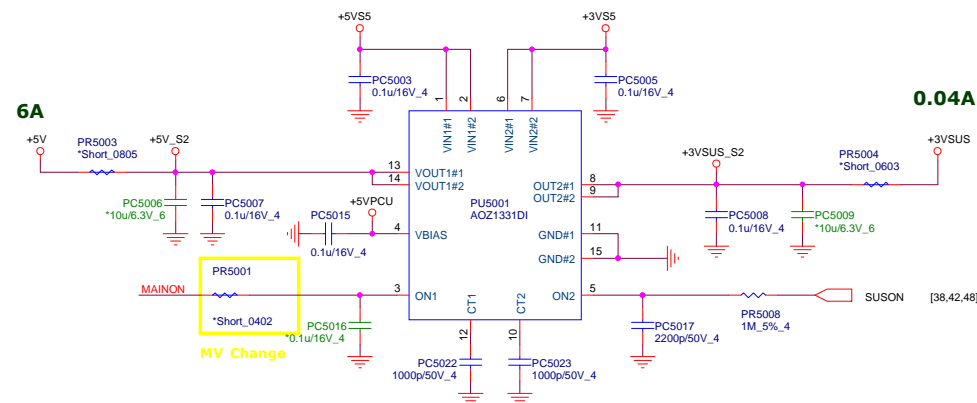
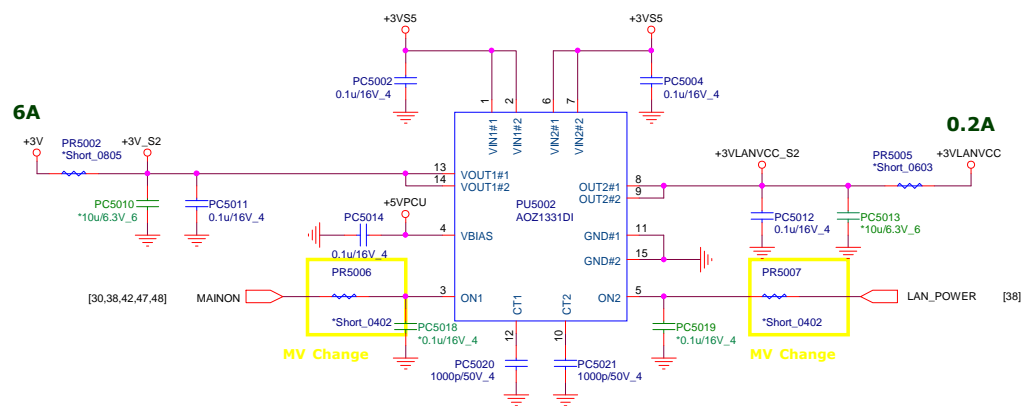
**PROJECT : G75C**  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	<b>+VCC_CORE (ISL95808HRZ-T)</b>	2A
Date:	Wednesday, March 08, 2017	Sheet 44 of 52




**PROJECT : G75C**  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	<b>+VCCGT/SA (ISL95808HRZ-T)</b>	1A
Date: Wednesday, March 08, 2017	Sheet 45 of 52	

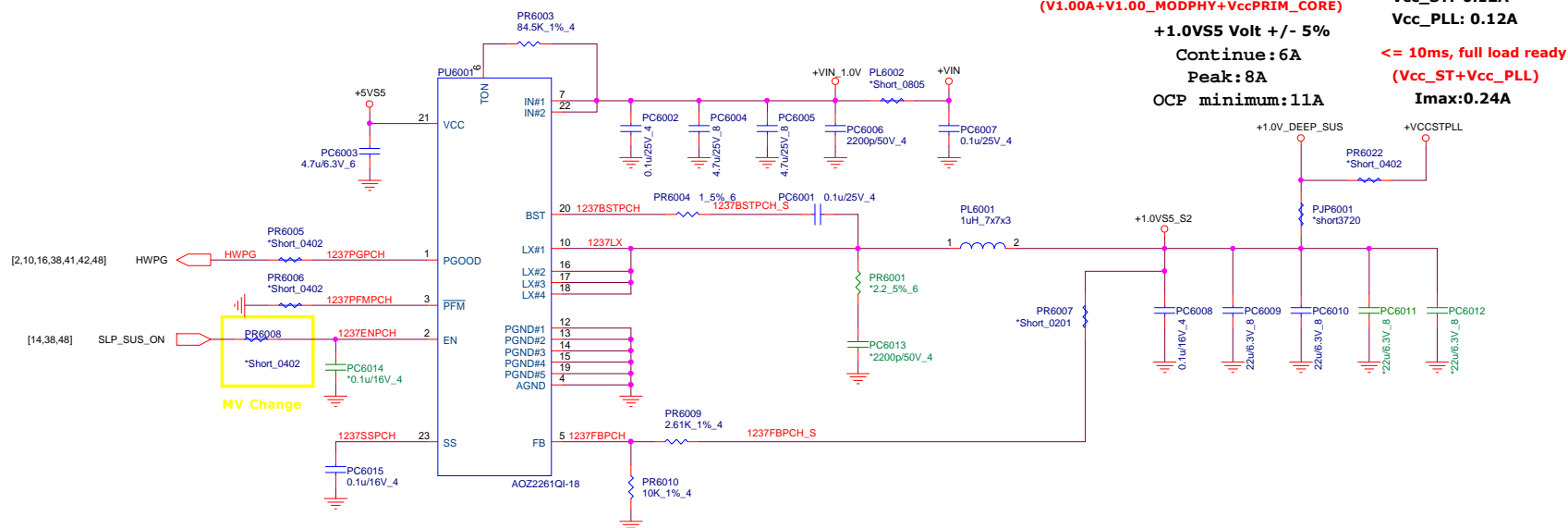


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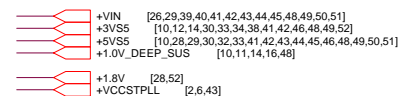
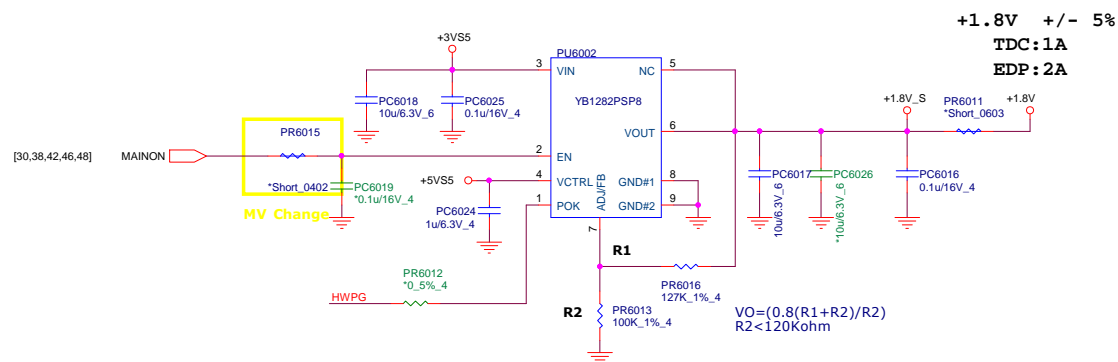
+3V	[5,9,10,11,12,13,14,16,17,18,19,26,28,29,30,34,35,36,37,38,39,43]
+5V	[26,27,28,29,34,35,39]
+3VS5	[10,12,14,30,33,34,38,41,42,47,48,49,52]
+5VS5	[10,28,29,30,32,33,41,42,43,44,45,47,48,49,50,51]
+3VSUS	[39]
+3VLANVCC	[36]
+5V_CAM	[36]
+3V_DEEP_SUS	[9,10,12,13,14,16,18]

	<b>PROJECT : G75C</b> Quanta Computer Inc.	
	Size Custom Document Number <b>Load switch IC (AOZ1331D)</b>	Rev 1A
Date: Wednesday, March 08, 2017   Sheet 46 of 52		





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**PROJECT : G75C**  
Quanta Computer Inc.

Size Custom	Document Number <b>+1.0_DEEP_SUS</b>	Rev 2A
Date: Wednesday, March 08, 2017	Sheet 47 of 52	

## Volume Segment

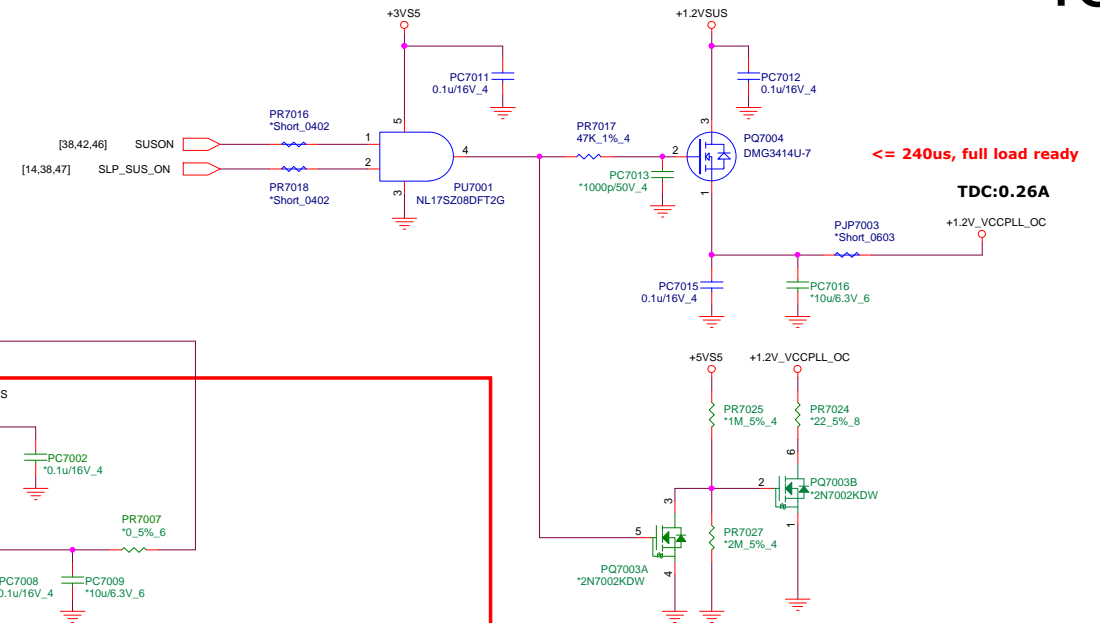
Vcc\_STG: 0.04A

Vcc\_IO: 5.5A

&lt;= 10ms full load ready

Imax:5.5A

Imax:0.04A



Reserve for separating +1.0V and VCCIO

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+0.95 +/- 5%  
Continue:4A  
Peak:5.5A  
OCP minimum:8A

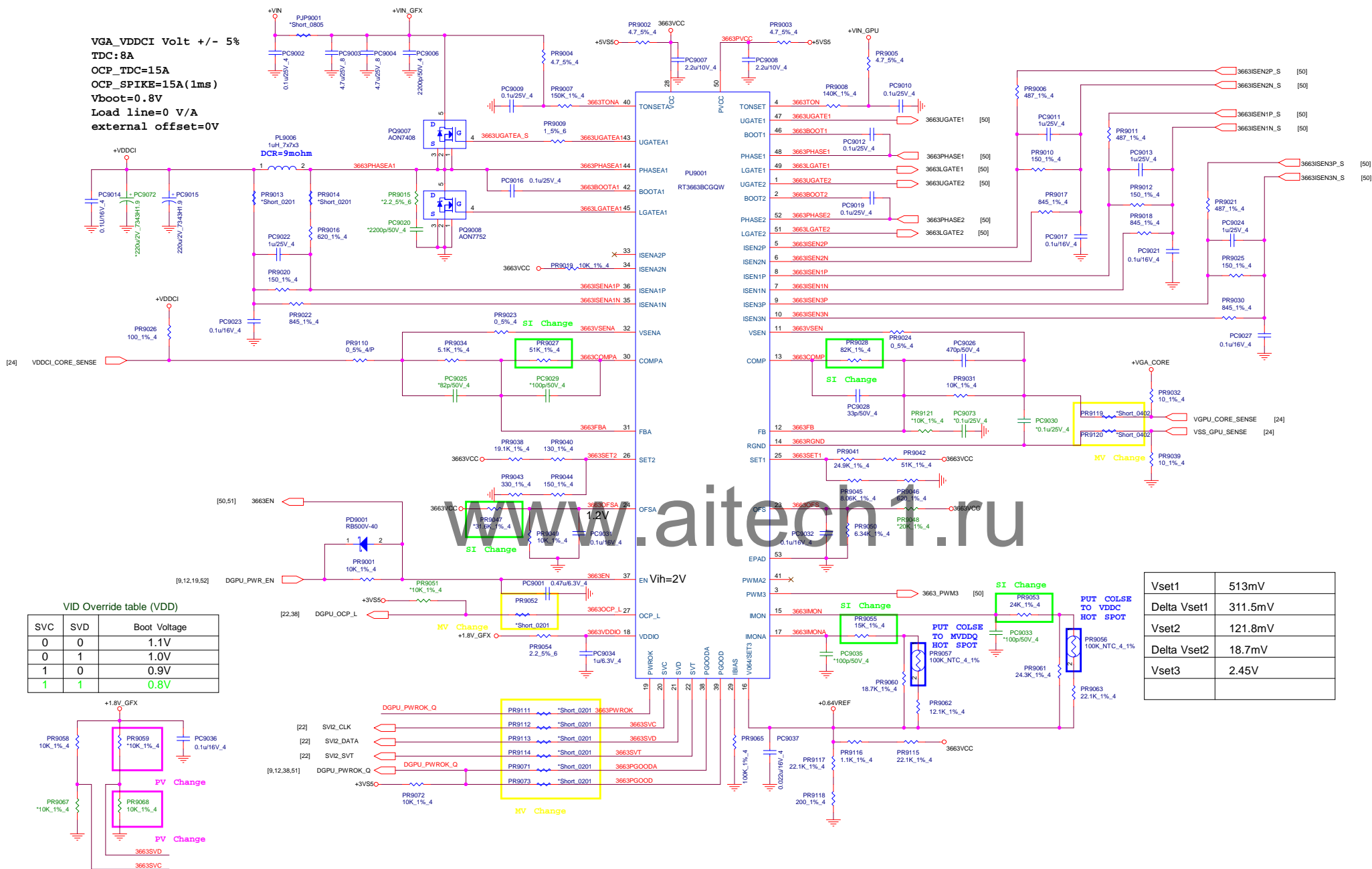
+1.0V	[2,5,6,10,16,38]
+3V5S	[10,12,14,30,33,34,38,41,42,46,47,49,52]
+5V5S	[10,28,29,30,32,33,41,42,43,44,45,46,47,49,50,51]
+VCCIO	[3,6,16]
+1.0V_DEEP_SUS	[10,11,14,16,47]
+1.2V_VCCPLL_OC	[6]
+1.2V_SUS	[2,6,10,17,18,42]



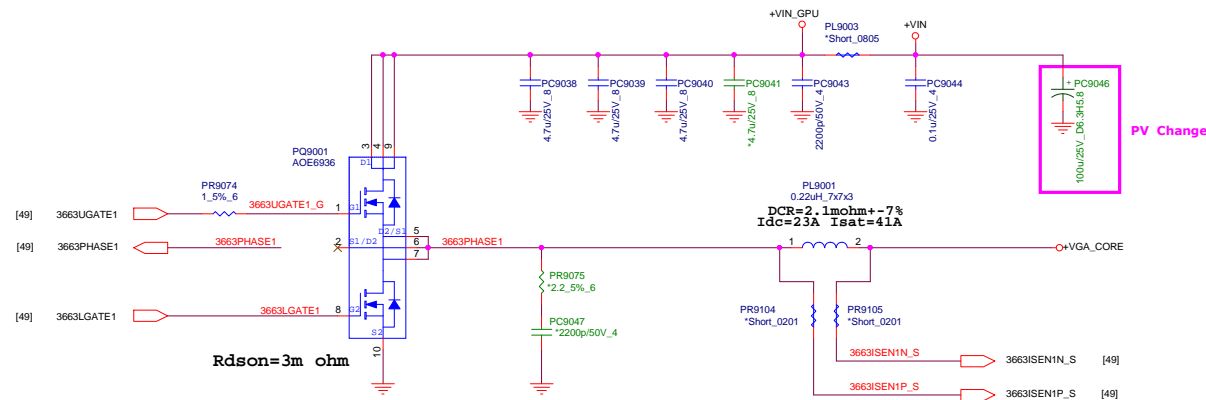
**PROJECT : G75C**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<b>+1.0V/+VCCSTPLL/+VCCIO</b>	1A
Date: Wednesday, March 08, 2017	Sheet 48 of 52	

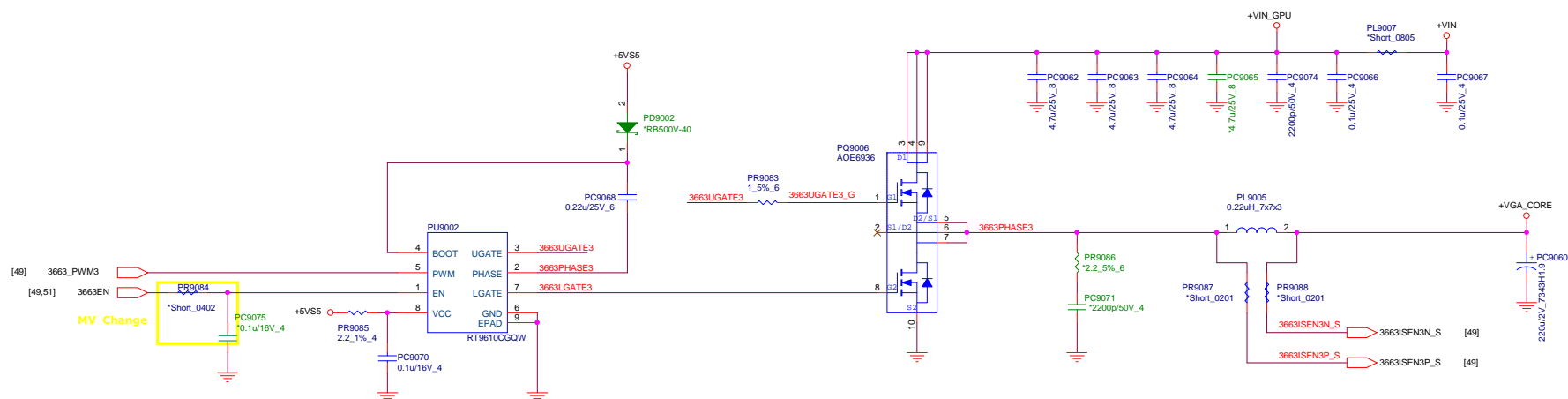
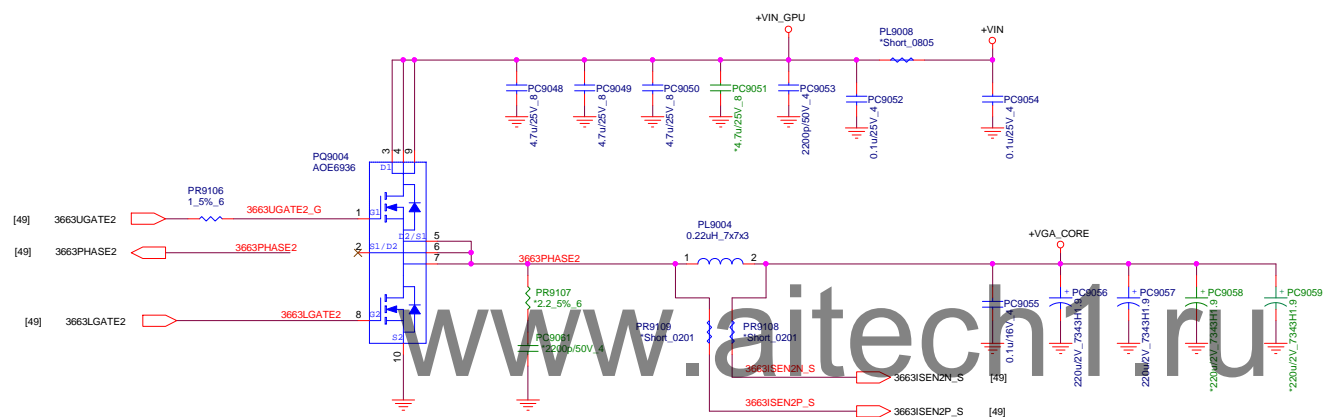
```
VGA_VDDCI Volt +/- 5%
TDC:8A
OCP_TDC=15A
OCP_SPIKE=15A(1ms)
Vboot=0.8V
Load line=0 V/A
external offset=0V
```

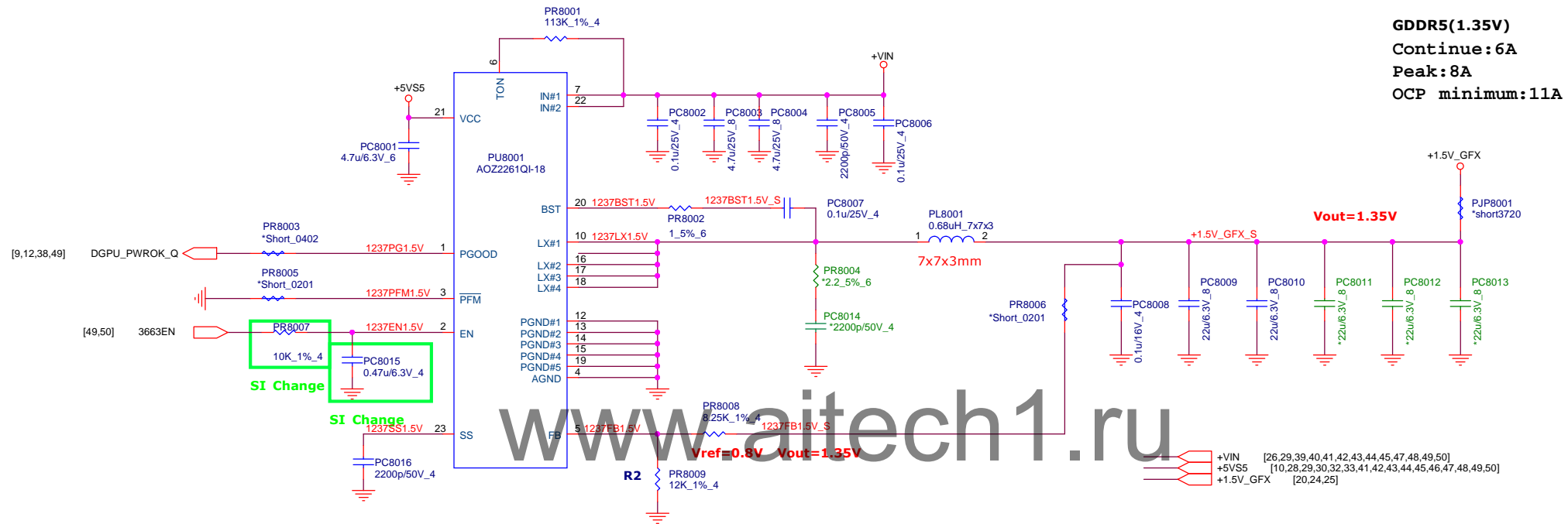


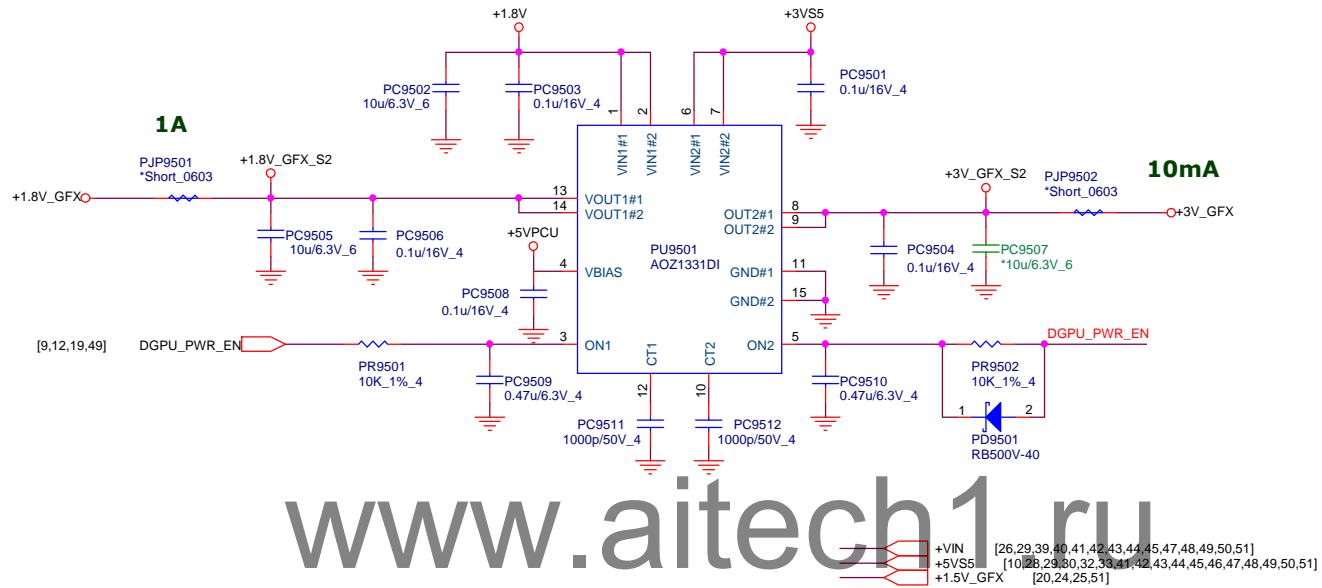
Vset1	513mV
Delta Vset1	311.5mV
Vset2	121.8mV
Delta Vset2	18.7mV
Vset3	2.45V



```
VGACORE ( R17M P1-70 40W )
Countinue current:47A
EDC=80A
OCP_TDC=90A
OCP_SPIKE=120A(1ms)
Per phase OCP=A
Vboot=0.8V
LL=0.6m V/A
external offset=0V
```







**PROJECT : G75C**  
Quanta Computer Inc.

Size B	Document Number <b>EC ENE KB9027B</b>	Rev 1A
Date: Wednesday, March 08, 2017   Sheet 52 of 52		